High Performance, Low Power, ISM Band FSK/GFSK/OOK/MSK/GMSK Transceiver IC

Preliminary Technical Data

ADF7023

FEATURES

- Ultra low power, high performance transceiver IC
- Frequency bands
  - 862 MHz to 928 MHz
  - 431 MHz to 464 MHz
- Data rates supported
  - 1 kbps to 300 kbps
- 1.8 V to 3.6 V power supply
- Single-ended and differential PAs
- Low IF receiver with programmable IF bandwidths
  - 100kHz, 150kHz, 200kHz, 300kHz
- Receiver sensitivity (BER)
  - –116 dBm at 1.0 kbps, 2FSK, GFSK
  - –107.5 dBm at 38.4 kbps, 2FSK, GFSK
  - –102.5 dBm at 150 kbps, GFSK, GMSK
  - –100 dBm at 300 kbps, GFSK, GMSK
  - –104 dBm at 19.2 kbps, OOK
- Very low power consumption
  - 12.8mA in PHY_RX mode (Max front-end gain)
  - 24.1mA in PHY_TX mode (10dBm output, single-ended PA)
  - 0.65 µA in PHY_SLEEP Mode (RC oscillator active)
  - 0.3 uA in PHY_SLEEP Mode (Deep Sleep Mode 1)
- RF output power of -20dBm to +13.5dBm (single-ended PA)
- RF output power of -20dBm to +10dBm (differential PA)
- Patented fast settling automatic frequency control (AFC)
- Digital received signal strength indication (RSSI)
- Integrated PLL loop filter and Tx/Rx switch
- Fast automatic VCO calibration
- Automatic synthesizer bandwidth optimization
- On-chip, low-power, custom 8-bit processor performs:
  - Radio Control
  - Packet Handling
  - Smart Wake Mode
- Packet management support
  - Highly flexible for a wide range of packet formats
  - Insertion/detection of Preamble/SWD/CRC/Address
  - Manchester/8b10b data encoding and decoding
  - Data Whitening
- Smart wake mode
  - Current saving low power mode with autonomous receiver wake up, carrier sense and packet reception
- Downloadable firmware modules
  - Image rejection calibration, fully automated (patent pending)
  - 128-bit AES encryption/decryption with hardware acceleration and key sizes of 128,192 or 256 bits
  - Reed-Solomon error correction with hardware acceleration
- 240 byte Packet Buffer for TX/RX data
- Efficient SPI control interface with block read/write access
- Integrated battery alarm and temperature sensor
- Integrated RC and 32.768kHz crystal oscillator
- On-chip 8-bit ADC
- 5 x 5 mm, 32 pin, LFCSP package

APPLICATIONS

- Smart Metering
- IEEE 802.15.4g
- Wireless MBUS
- Home Automation
- Process and Building Control
- Wireless Sensor Networks (WSNs)
- Wireless Healthcare

Rev. PrF

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FUNCTIONAL BLOCK DIAGRAM

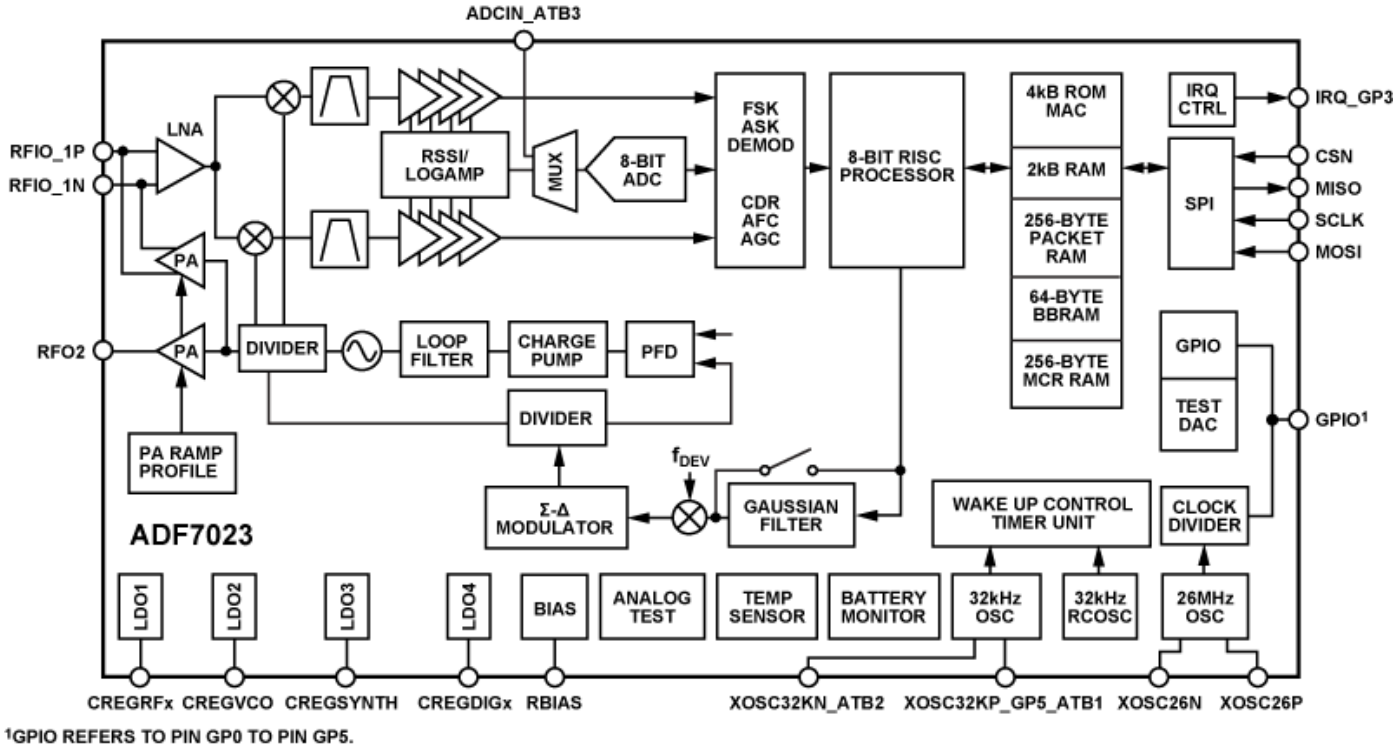

Figure 1.

TERMINOLOGY

ADC	Analog to Digital Converter
AGC	Automatic Gain Control
AFC	Automatic Frequency Control
Battmon	Battery Monitor
BBRAM	Battery Back-up Random Access Memory
CRC	Cyclic Redundancy Check
DR	Data Rate
FSK	Two level Frequency Shift Keying
GFSK	Two level Gaussian Frequency Shift Keying
SWM	Smart Wake Mode
MCR	Modem Configuration RAM
MER	Modulation Error Rate
NOP	No Operation
OOK	On-Off Keying
PA	Power Amplifier
PFD	Phase Frequency Detector
PHY	Physical Layer
RCO	RC Oscillator
RISC	Reduced Instruction Set Computer
RSSI	Receive Signal Strength Indicator
Rx	Receive
SWD	Sync Word Detect
SWM	Smart Wake Mode
Tx	Transmit
VCO	Voltage Controlled Oscillator
WUC	Wake Up Controller
XOSC	Crystal Oscillator

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GENERAL DESCRIPTION

The ADF7023 is a very low power, high performance, highly integrated FSK/GFSK/OOK/MSK/GMSK transceiver designed for operation in the frequency bands, 862MHz to 928MHz and 431MHz to 464MHz, which cover the worldwide license-free ISM bands at 433 MHz, 868 MHz and 915 MHz. It is suitable for circuit applications that operate under the European ETSI EN300-220, the North American FCC (Part 15), the Chinese short range wireless regulatory standards or other similar regional standards. Data rates from 1kbps to 300kbps are supported.

The transmit RF synthesizer contains a VCO and a low noise fractional-N PLL with an output channel frequency resolution of 400Hz. The VCO operates at 2x or 4x the fundamental frequency to reduce spurious emissions. The receive and transmit synthesizer bandwidths are automatically, and independently, configured to achieve optimum phase noise, modulation quality and settling time. The transmitter output power is programmable from −20 dBm to +13.5 dBm, with automatic PA ramping to meet transient spurious specifications. The part possesses both single-ended and differential PAs, which allow for Tx antenna diversity.

The receiver is exceptionally linear, achieving an IP3 specification of −12.2 dBm and −11.5 dBm at maximum gain and minimum gain, respectively. Thus, the part is extremely resilient to the presence of interferers in spectrally noisy environments. The receiver features a novel, high speed automatic frequency control (AFC) loop, allowing the PLL to find and correct any RF frequency errors in the recovered packet. A patent pending, image rejection calibration scheme is available through a program download. The algorithm does not require the use of an external RF source, nor does it require any user intervention once initiated. The results of the calibration can be stored in non-volatile memory for use on subsequent power ups of the transceiver.

The ADF7023 operates with a power supply range of 1.8 V to 3.6 V and has very low power consumption in both Tx and Rx modes enabling long lifetimes in battery operated systems while maintaining excellent RF performance. The device can enter a low power sleep mode in which the configuration settings are retained in BBRAM.

The ADF7023 features an ultra low power, on-chip, communications processor. The communications processor, which is custom RISC, 8-bit processor, performs the radio control, packet handling and smart wake mode (SWM) functionality. The communications processor eases the processing burden of the companion microprocessor by integrating the lower layers of a typical communication protocol stack. The communications processor also permits the download and execution of a set of firmware modules which include image rejection (IR) calibration, AES encryption and Reed Solomon coding.

The communications processor provides a simple command based radio control interface for the host microprocessor. A single byte command transitions the radio between states or performs a radio function.

The communications processor provides support for a generic payload format. The packet format is highly flexible and fully programmable, thereby ensuring it is compatible with proprietary packet profiles. In transmit mode the communications processor can be configured to add preamble, sync word and CRC to the payload data stored in packet RAM. In receive mode the communications processor can detect and interrupt the MCU on reception of preamble, sync word, address and CRC and store the received payload to packet RAM. The ADF7023 utilises an efficient interrupt system comprising of MAC level Interrupts and PHY level interrupts that can be individually set.The payload data plus the 16-bit CRC can be encoded/decoded using Manchester or 8b/10b encoding. Alternatively, data whitening and de-whitening can be applied.

The smart wake mode (SWM) allows the ADF7023 to wake up autonomously from sleep using the internal wake-up timer without intervention from the host microprocessor. After wake-up the ADF7023 is controlled by the communications processor. This functionality allows carrier sense, packet sniffing and packet reception while the host microprocessor is in sleep, thereby reducing overall system current consumption. The smart wake mode can wake the host microprocessor on an interrupt condition. These interrupt conditions can be configured to include the reception of valid preamble, sync word, CRC, or address match. Wake up from sleep mode can also be triggered by the host microprocessor. For systems requiring very accurate wake-up timing a 32kHz oscillator can be used to drive the wake up timer. Alternatively, the internal RC oscillator can be used, which gives lower current consumption in sleep.

The ADF7023 features an Advanced Encryption Standard (AES) engine with hardware acceleration that provides 128-bit block encryption and decryption with key sizes of 128, 192 and 256 bits. Both Electronic Code Book (ECB) and Cipher Block Chaining Mode 1 (CBC Mode 1) are supported. The AES engine can be used to encrypt/decrypt packet data but can also be used as a stand-alone engine for encryption/decryption by the host microprocessor. The AES engine is enabled on the ADF7023 by downloading the AES software module to program RAM. The AES software module is available from Analog Devices.

An on-chip 8-bit ADC provides readback of an external analog input, the RSSI signal, or an integrated temperature sensor. An integrated battery voltage monitor raises an interrupt flag to the host microprocessor whenever the battery voltage drops below a user defined threshold.

SPECIFICATIONS

V_{DD} = 1.8V to 3.6 V, GND = 0 V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical specifications are at V_{DD} = 3 V, T_A = 25°C.

RF AND SYNTHESIZER SPECIFICATIONS

Table 1

Parameter	Min	Typ	Max	Unit	Test Conditions
RF CHARACTERISTICS					
Frequency Ranges	862		928	MHz	
	431		464	MHz	
PHASE-LOCKED LOOP					
Channel freq resolution					
Phase Noise (In-Band)		–88		dBc/Hz	10 kHz offset, PA output power = 10 dBm, RF = 868MHz
Phase Noise at offset of					
1MHz		-126		dBc/Hz	PA output power= 10 dBm, RF = 868 MHz
2MHz		-131		dBc/Hz	PA output power = 10 dBm, RF = 868 MHz
10MHz		-142		dBc/Hz	PA output power = 10 dBm, RF = 868 MHz
Clock-Related Spur Level		60		dBc	Measured in a span of ±350 MHz for synthesizer bandwidth =92kHz, PA output power = 10 dBm, V_{DD} = 3.6 V, single-ended PA used
VCO Calibration Time		142		µs	
Synthesizer Settling Time in					Frequency synthesizer settles to within ±5 ppm of the target frequency within this time following the VCO calibration.
Receive		56		µs	All data rates and modulation
Transmit		TBD		µs	FSK/MSK/GFSK, Data rate = 0.1 to 49.6kbps
Transmit		56		µs	FSK/MSK/GFSK, Data rate = 49.7 to 99.2kbps
Transmit		TBD		µs	FSK/MSK/GFSK, Data rate = 99.3 to 129.6kbps
Transmit		TBD		µs	FSK/MSK/GFSK, Data rate = 129.7 to 179.2kbps
Transmit		TBD		µs	FSK/MSK/GFSK, Data rate = 179.3 to 240kbps
Transmit		TBD		µs	FSK/MSK/GFSK, Data rate = 240.1 to 300kbps
Transmit		TBD		µs	OOK, all data rates
CRYSTAL OSCILLATOR					
Crystal Frequency		26		MHz	Parallel load resonant crystal
Recommended Load Capacitance	7		18	pF	
Maximum Crystal ESR		1800		Ω	26 MHz crystal with 18 pF load capacitance
Parasitic Capacitance		TBD			
Start-Up Time		310		µs	26 MHz crystal with 7 pF load capacitance
		388		µs	26 MHz crystal with 18 pF load capacitance
SPURIOUS EMISSIONS					
Integer Boundary Spurious					
910.1MHz		TBD		dBc	using 92khz synthesizer bandwidth, integer boundary spur at 910MHz (= 26MHz × 35)
911.0MHz		TBD		dBc	using 92khz synthesizer bandwidth,, integer boundary spur at 910MHz (= 26MHz × 35)
Reference Spurious					
915Mhz		TBD		dBc	using 92khz synthesizer bandwidth,
868MHz		TBD		dBc	using 92khz synthesizer bandwidth,

TRANSMITTER SPECIFICATIONS

Table 2

Parameter	Min	Typ	Max	Unit	Test Conditions
DATA RATE					
2FSK/GFSK/MSK/GMSK	1		300	kbps	
OOK	TBD		19.2	kbps	Manchester encoding enabled (Manchester chip rate = 2 x data rate)
Data Rate Resolution		100		bps	
Modulation Error Rate (MER)					
1 to 49.6 kbps data rate		TBD		dB	FSK
49.7 to 99.2kbps data rate		TBD		dB	FSK
99.3 to 129.6kbps data rate		TBD		dB	FSK
129.7 to 179.2kbps data rate		TBD		dB	GFSK
179.3 to 240kbps data rate		TBD		dB	GFSK
240.1 to 300kbps data rate		TBD		dB	GFSK
MODULATION					
2FSK/GFSK Frequency Deviation	0.1		409.5	kHz	
Deviation Frequency Resolution		100		Hz	
Gaussian Filter BT		0.5			non-programmable
OOK					
PA Off Feedthrough		-94		dBm	
VCO Frequency Pulling		30		kHz rms	Data rate = 19.2kbps (38.4 kcps Manchester encoded), PA output = 10dBm, PA ramp rate = 64 codes/bit
SINGLE-ENDED PA					
Maximum Power[1]		13.5		dBm	Programmable, separate PA and LNA match[2]
Minimum Power		-20		dBm	
Transmit Power Variation vs. temperature		±0.5		dB	From −40°C to +85°C, RF Frequency = 868 MHz
Transmit Power Variation vs. VDD		±1		dB	From 1.8 V to 3.6 V, RF Frequency = 868 MHz
Transmit Power Flatness		±1		dB	From 902 MHz to 928 MHz and 863MHz to 870MHz
Programmable Step Size					
−20 dBm to +13.5 dBm		0.5		dB	programmable in 63 steps
DIFFERNETIAL PA					
Maximum Power[1]		10		dBm	Programmable
Minimum Power		-20		dBm	
Transmit Power Variation vs. temperature		±1		dB	From −40°C to +85°C, RF Frequency = 868 MHz
Transmit Power Variation vs. VDD		±2		dB	From 1.8 V to 3.6 V, RF Frequency = 868 MHz
Transmit Power Flatness		±1		dB	From 863 MHz to 870 MHz
Programmable Step Size					
−20 dBm to +10 dBm		0.5		dB	programmable in 63 steps
HARMONICS					868MHz, Unfiltered conductive, PA output power = 10dBm
Single-ended PA					
Second Harmonic		-15.1		dBc	
Third Harmonic		-29.3		dBc	
All Other Harmonics		-47.6		dBc	
Differential PA					
Second Harmonic		-23.2		dBc	
Third Harmonic		-25.2		dBc	
All Other Harmonics		-24.2		dBc	
OPTIMUM PA LOAD IMPEDANCE					

Single-ended PA, in transmit mode			
f_{RF} = 915 MHz	46.9 +j0.2	Ω	
f_{RF} = 868 MHz	38.0 +j17.2	Ω	
f_{RF} = 433 MHz	TBD	Ω	
Single-ended PA, in receive mode			
f_{RF} = 915 MHz	9.4 -j124	Ω	
f_{RF} = 868 MHz	9.5 -j130.6	Ω	
f_{RF} = 433 MHz	11.9 -j260.1	Ω	
Differential PA, in transmit mode			Load impedance between RFIO_1P and RFIO_1N to ensure maximum power transfer
f_{RF} = 915 MHz	56.8+j92.2	Ω	
f_{RF} = 868 MHz	66.3+j56.1	Ω	
f_{RF} = 433 MHz	98.2+j7.2	Ω	

[1] Measured as the maximum un-modulated power.
[2] A combined single-ended PA and LNA match can reduce the maximum achievable output power by up to 1dB.

RECEIVER SPECIFICATIONS

Table 3

Parameter	Min	Typ	Max	Unit	Test Conditions
2FSK/GFSK INPUT SENSITIVTY , Bit Error Rate (BER)					At BER = 1E – 3, RF Frequency = 868 MHz, 915MHz LNA and PA matched separately[1]
1.0 kbps		-116		dBm	Frequency Deviation = 4.8kHz, IF Filter Bandwidth = 100kHz
10 kbps		-111		dBm	Frequency Deviation = 9.6kHz, IF Filter Bandwidth = 100kHz
38.4 kbps		-107.5		dBm	Frequency Deviation = 20kHz, IF Filter Bandwidth = 100kHz
38.4 kbps		TBD		dBm	Frequency Deviation = 50kHz, IF Filter Bandwidth = 100kHz
50 kbps		-106.3		dBm	Frequency Deviation = 12.5kHz, IF Filter Bandwidth = 100kHz
100 kbps		-103.7		dBm	Frequency Deviation = 25kHz, IF Filter Bandwidth = 100kHz
100kbps		TBD		dBm	Frequency Deviation = 50kHz, IF Filter Bandwidth = 150kHz
150 kbps		-102.5		dBm	Frequency Deviation = 37.5kHz, IF Filter Bandwidth = 150kHz
200 kbps		-101		dBm	Frequency Deviation = 50kHz, IF Filter Bandwidth = 200kHz
300 kbps		-100		dBm	Frequency Deviation = 75 kHz, IF Filter Bandwidth = 300kHz
2FSK/GFSK INPUT SENSITIVTY , Packet Error Rate (PER)					At PER = 1%, RF Frequency = 868 MHz, 915MHz LNA and PA matched separately[2], packet length =128 bits, packet mode.
1.0 kbps		-114		dBm	Frequency Deviation = 4.8kHz, IF Filter Bandwidth = 100kHz
9.6 kbps		-109		dBm	Frequency Deviation = 9.6kHz, IF Filter Bandwidth = 100kHz
38.4 kbps		-106		dBm	Frequency Deviation = 20kHz, IF Filter Bandwidth = 100kHz
38.4 kbps		TBD		dBm	Frequency Deviation = 50kHz, IF Filter Bandwidth = 100kHz
50 kbps		-104.3		dBm	Frequency Deviation = 12.5kHz, IF Filter Bandwidth = 100kHz
100 kbps		-101.7		dBm	Frequency Deviation = 25kHz, IF Filter Bandwidth = 100kHz
100kbps		TBD		dBm	Frequency Deviation = 50kHz, IF Filter Bandwidth = 150kHz
150 kbps		-100.5		dBm	Frequency Deviation = 37.5kHz, IF Filter Bandwidth = 150kHz
200 kbps		-99		dBm	Frequency Deviation = 50kHz, IF Filter Bandwidth = 200kHz
300 kbps		-98		dBm	Frequency Deviation = 75 kHz, IF Filter Bandwidth = 300kHz
OOK INPUT SENSITIVITY					At BER = 1E – 3, RF Frequency = 868 MHz, LNA and PA matched separately[1]
Sensitivity at 19.2kbps, (38.4 kcps, Manchester encoded)		-104		dBm	IF Filter Bandwidth = 100kHz
LNA AND MIXER, INPUT IP3					f_{RF} = 868.25 MHz, $f_{SOURCE1} = f_{RF} + 1.1$ MHz, $f_{SOURCE2} = f_{RF} + 2$ MHz
Min LNA gain		-11.5		dBm	
Max LNA gain		-12.2		dBm	
1dB COMPRESSION POINT		-22.4		dBm	Max LNA gain
ADJACENT CHANNEL REJECTION					

CW Interferer			Wanted signal 3 dB above the input sensitivity level (BER = 10^{-2}), CW interferer power level increased until BER = 10^{-2}.As per ETSI EN300-220.
150kHz channel spacing	TBD	dB	IF BW = 100 kHz, Wanted signal: Fdev = 19.2kHz, DR=38.4kbps, GFSK, Level = TBD
200kHz channel spacing	37	dB	IF BW = 100 kHz, Wanted signal: Fdev = 19.2kHz, DR=38.4kbps, GFSK, Level = TBD
200kHz channel spacing	TBD	dB	IF BW = 150 kHz, Wanted signal: Fdev = 25kHz, DR=50kbps, GFSK, Level = TBD
300kHz channel spacing	TBD	dB	IF BW = 200 kHz, Wanted signal: Fdev = 50kHz, DR=150kbps, GFSK, Level = TBD
400kHz channel spacing	TBD	dB	IF BW = 200 kHz, Wanted signal: Fdev = 50kHz, DR=150kbps, GFSK, Level = TBD
500kHz channel spacing	TBD	dB	IF BW = 300 kHz, Wanted signal: Fdev = 50kHz, DR=200kbps, GFSK, Level = TBD
Modulated Interferer			Wanted signal 3 dB above the input sensitivity level (BER = 10^{-2}), Modulated interferer, power level increased until BER = 10^{-2}.
150kHz channel spacing	TBD	dB	IF BW = 100 kHz, Wanted/Interferer signal: Fdev = 19.2kHz, DR=38.4kbps, GFSK, Wanted Level = TBD
200kHz channel spacing	TBD	dB	IF BW = 100 kHz, Wanted/Interferer signal: Fdev = 19.2kHz, DR=38.4kbps, GFSK, Wanted Level = TBD
200kHz channel spacing	TBD	dB	IF BW = 150 kHz, Wanted/Interferer signal: Fdev = 25kHz, DR=50kbps, GFSK, Wanted Level = TBD
300kHz channel spacing	TBD	dB	IF BW = 200 kHz, Wanted/Interferer signal: Fdev = 50kHz, DR=150kbps, GFSK, Wanted Level = TBD
400kHz channel spacing	TBD	dB	IF BW = 200 kHz, Wanted/Interferer signal: Fdev = 50kHz, DR=150kbps, GFSK, Wanted Level = TBD
500kHz channel spacing	TBD	dB	IF BW = 300 kHz, Wanted/Interferer signal: Fdev = 50kHz, DR=200kbps, GFSK, Wanted Level = TBD
CO-CHANNEL REJECTION	-4	dB	Desired signal 10 dB above the input sensitivity level (BER = 10^{-3}). Data rate = 38.4kbps, frequency deviation = 20kHz.
BLOCKING			Desired signal 3 dB above the input sensitivity level (BER = 10^{-2}) of -107.5dBm. Modulated interferer power level increased until BER = 10^{-2}. (refer to typical performance curves for blocking at other offsets)
±2 MHz	66	dB	
±10 MHz	73	dB	
WIDEBAND INTERFERENCE REJECTION	75	dB	RF Frequency = 868 MHz, swept from 10MHz to 100MHz either side of RF Frequency.
IMAGE CHANNEL REJECTION			Measured as image attenuation at the IF filter output. Carrier wave interferer at 400kHz below the channel frequency. 100kHz IF Filter bandwidth, 868MHz.
915MHz	TBD/TBD	dB	Uncalibrated/Calibrated
868MHz	27/45	dB	Uncalibrated/Calibrated
433MHz	TBD/TBD	dB	Uncalibrated/Calibrated
AFC			
Accuracy	1	kHz	
Maximum Pull-In Range			Achievable pull in range depends on discriminator bandwidth and modulation.
300kHz IF filter bandwidth	±150	kHz	
200kHz IF filter bandwidth	±100	kHz	
150kHz IF filter bandwidth	±75	kHz	
100kHz IF filter bandwidth	±50	kHz	
Preamble			Minimum number of bits to ensure preamble detection.
Minimum number of bits, AFC off			

38.4 kbps	16	bits	Frequency deviation = 20 kHz
100 kbps	TBD	bits	
200 kbps	TBD	bits	
300 kbps	TBD	bits	
Minimum number of bits, AFC on			
38.4 kbps	35	bits	
100 kbps	TBD	bits	
200 kbps	TBD	bits	
300 kbps	TBD	bits	
RSSI			
Range at Input	−97 to −26	dBm	
Linearity	±2	dB	
Absolute Accuracy	±3	dB	
Response Time	150	µs	
Saturation (Maximum Input Level)			
FSK/GFSK	12	dBm	
OOK	-10	dBm	
LNA INPUT IMPEDANCE			
Receive mode			
f_{RF} = 915 MHz	73.6 -j34.6	Ω	
f_{RF} = 868 MHz	75.8 -j34.2	Ω	
f_{RF} = 433 MHz	95.9 -j24.1	Ω	
Transmit mode			
f_{RF} = 915 MHz	7.4+j8.6	Ω	
f_{RF} = 868 MHz	7.5+j8.2	Ω	
f_{RF} = 433 MHz	7.6+j4.9	Ω	
RX SPURIOUS EMISSIONS[3]			
Maximum <1 GHz	−57	dBm	at antenna input, unfiltered conductive
Maximum >1 GHz	−47	dBm	at antenna input, unfiltered conductive

[1] Sensitivity for combined matching network case is typically 1 dB less than separate matching networks.
[2] Sensitivity for combined matching network case is typically 1 dB less than separate matching networks.
[3] Follow the matching and layout guidelines to achieve the relevant FCC/ETSI specifications.

TIMING AND DIGITAL SPECIFICATIONS

Table 4

Parameter	Min	Typ	Max	Unit	Test Conditions
RX and TX TIMING PARAMETERS					
PHY_ON to PHY_RX (on CMD_PHY_RX)		300		us	includes VCO calibration and synthesizer settling
PHY_ON to PHY_TX (on CMD_PHY_TX)		300		us	includes VCO calibration and synthesizer settling, does not include PA ramp up
PHY_TX to PHY_RX (on CMD_PHY_RX)		300		us	includes VCO calibration and synthesizer settling
PHY_RX to PHY_TX (on CMD_PHY_TX)		300		us	includes VCO calibration and synthesizer settling, does not include PA ramp up
PHY_TX to PHY_RX (on auto turnaround)		50		us	does not include VCO calibration
PHY_RX to PHY_TX (on auto turnaround)		50		us	does not include PA ramp up and VCO calibration
LOGIC INPUTS					
Input High Voltage, V_{INH}	$0.7 \times V_{DD}$			V	
Input Low Voltage, V_{INL}			$0.2 \times V_{DD}$	V	
Input Current, I_{INH}/I_{INL}			±1	µA	
Input Capacitance, C_{IN}			10	pF	
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	$DV_{DD} - 0.4$			V	I_{OH} = 500 µA
Output Low Voltage, V_{OL}			0.4	V	I_{OL} = 500 µA
GPIO Rise/Fall			5	ns	
GPIO Load			10	pF	
Maximum Output Current		TBD		mA	
ATB OUTPUTS					
Output High Voltage, V_{OH}	TBD			V	I_{OH} = 500 µA
Output Low Voltage, V_{OL}			TBD	V	I_{OL} = 500 µA
Maximum Output Current		TBD		mA	

AUXILARY BLOCK SPECIFICATIONS

Table 5

RC OSCILLATOR				
Frequency		32.768	kHz	after calibration
Frequency accuracy		TBD	ppm	after calibration
32kHz XTAL OSCILLATOR				
Frequency		32.768	kHz	
Frequency accuracy		±1	ppm	
Start-up time		630	ms	32.768 kHz crystal with 7 pF load capacitance
WAKE UP CONTROLLER (WUC)				
Hardware Timer				
Wake-up period	61×10^{-6}	1.31×10^{5}	sec	
Firmware Timer				
Wake-up period	1	2^{16}	Hardware periods	The firmware counter counts the number of hardware wake-ups and has a resolution of 16 bits
ADC				
Resolution		8	bits	
DNL		±1	LSB	From 1.8 V to 3.6 V, T_A = 25°C
INL		±1	LSB	From 1.8 V to 3.6 V, T_A = 25°C
Conversion time		1	µs	
Input Capacitance		12.4	pF	
BATTERY MONITOR				
Absolute Accuracy		±45	mV	
Alarm Voltage Set Point	1.7	2.7	V	
Alarm Voltage Step Size		62	mV	5-bit resolution
Start-Up Time		100	µs	
Current Consumption		30	µA	When enabled
TEMPERATURE SENSOR				
Range	−40	+85	°C	
Resolution		0.3	°C	With averaging
Accuracy of Temperature Readback				With a temperature correction value (determined at a known temperature) applied. From −40°C to +85°C
Single readback		±14	°C	
Average of 10 Readbacks		±4.4	°C	
Average of 50 Readbacks		±2	°C	

GENERAL SPECIFICATIONS

Table 6

TEMPERATURE RANGE, T_A	−40	+85	°C	
VOLTAGE SUPPLY				
V_{DD}	1.8	3.6	V	Applied to VDDBAT1 and VDDBAT2
TRANMSIT CURENT CONSUMPTION				In state PHY_TX. Single-ended PA is matched to 50 Ω, differential PA is matched to 100 Ω. Separate single-ended PA and LNA match. Combined differential PA and LNA match
Single-ended PA, 433MHz				
−20 dBm		TBD	mA	
−10 dBm		TBD	mA	
0 dBm		TBD	mA	
10 dBm		TBD	mA	
13 dBm		TBD	mA	
Differential PA, 433MHz				
−20 dBm		TBD	mA	
−10 dBm		TBD	mA	
0 dBm		TBD	mA	
5 dBm		TBD	mA	
10 dBm		TBD	mA	
Single-ended PA, 868/915 MHz				
−20 dBm		9.2	mA	
−10 dBm		10.3	mA	
0 dBm		13.3	mA	
10 dBm		24.1	mA	
13.5 dBm		32.1	mA	
Differential PA, 868/915 MHz				
−20 dBm		TBD	mA	
−10 dBm		TBD	mA	
0 dBm		TBD	mA	
5 dBm		TBD	mA	
10 dBm		TBD	mA	
POWER MODES				
PHY_SLEEP (Deep Sleep Mode 2)		0.15	µA	Sleep mode, wake-up configuration values (BBRAM) not retained
PHY_SLEEP (Deep Sleep Mode 1)		0.3	µA	Sleep mode, wake-up configuration values (BBRAM) retained
PHY_SLEEP (RCO Wake Mode)		0.65	µA	WUC active, RC Oscillator running, wake-up configuration values retained (BBRAM)
PHY_SLEEP (XTO Wake Mode)		1.25	µA	WUC active, 32kHz crystal running, wake-up configuration values retained (BBRAM)
PHY_OFF		1	mA	Device in PHY_OFF state. 26MHz oscillator running, digital and synthesizer regulators active, all register values retained
PHY_ON		1	mA	Device in PHY_ON state, 26MHz oscillator running, digital, synthesizer, VCO and RF regulators active, baseband filter calibration performed, all register values retained
PHY_RX		12.8	mA	Device in PHY_RX state
SMART WAKE MODE				Average current consumption
		TBD	µA	Autonomous reception every TBDs, with reception time of TBD ms, using RC oscillator
		TBD	µA	Autonomous reception every TBDs, with reception time of TBD ms, using RC oscillator

TIMING SPECIFICATIONS

V_{DD} = 3 V ± 10%, V_{GND} = 0 V, T_A = T_{MIN} to T_{MA}, unless otherwise noted.

Table 7. SPI Interface Timing

Parameter	Limit	Unit	Test Conditions/Comments
t_1	15	ns max	CSN falling edge to MISO setup time (TRX active)
t_2	85	ns min	CSN low to SCLK setup time
t_3	85	ns min	SCLK high time
t_4	85	ns min	SCLK low time
t_5	170	ns min	SCLK period
t_6	10	ns max	SCLK falling edge to MISO delay
t_7	5	ns min	MOSI to SCLK rising edge setup time
t_8	5	ns min	MOSI to SCLK rising edge hold time
t_9	85	ns min	SCLK falling edge to CSN hold time
t_{11}	270	ns min	CSN high time
t_{12}	310	µs typ	CSN low to MISO high wake-up time, 26 MHz crystal with 7 pF load capacitance, T_A = 25°C
t_{13}	20	ns max	SCLK rise time
t_{14}	20	ns max	SCLK fall time

Timing Diagrams

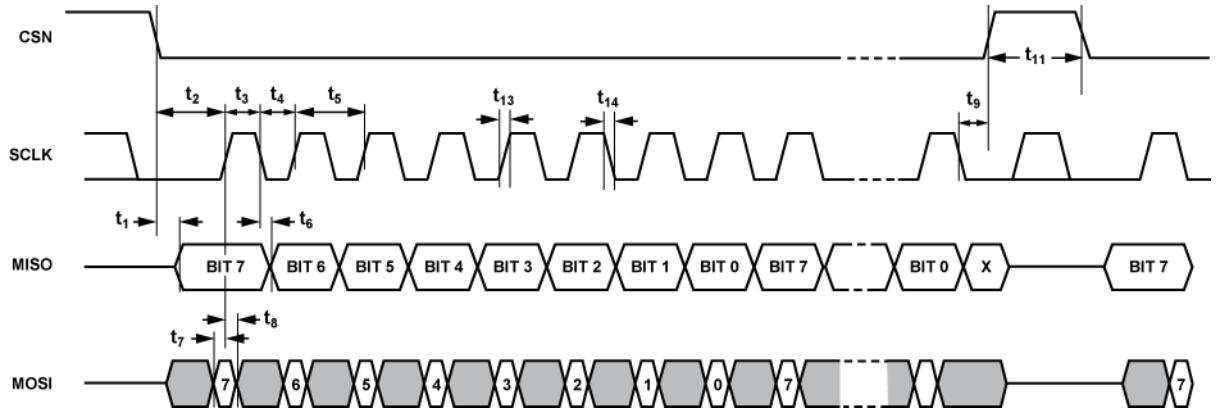


Figure 2. SPI Interface timing

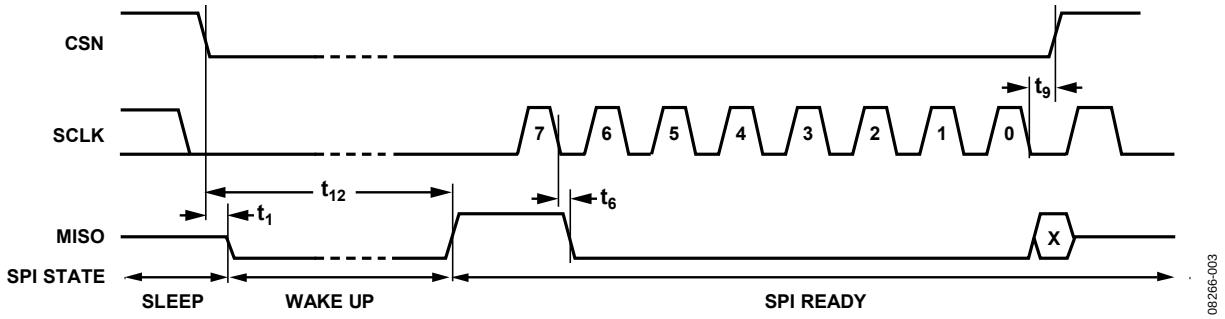


Figure 3. PHY_SLEEP to SPI Ready state timing (Note: SPI is ready t12 after falling edge of CSN)

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 8

Parameter	Rating
V_{DD} to GND	−0.3 V to +3.96 V
Operating Temperature Range	
Industrial	−40°C to +85°C
Storage Temperature Range	−65°C to +125°C
Maximum Junction Temperature	150°C
LFCSP θ_{JA} Thermal Impedance	26°C/W
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	40 sec

The exposed paddle of the LFCSP package should be connected to ground.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device is a high performance RF integrated circuit with an ESD rating of <2 kV, and it is ESD sensitive. Proper precautions should be taken for handling and assembly.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

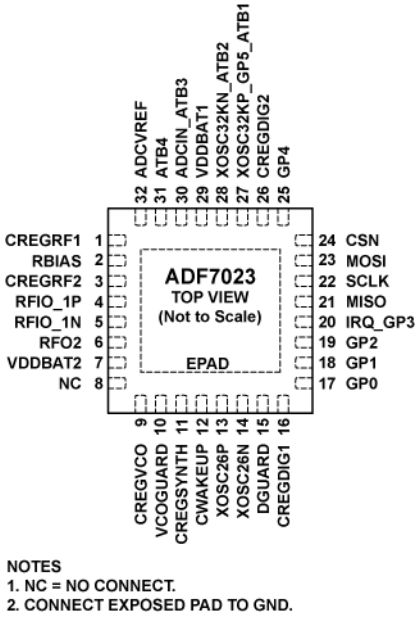


Figure 4. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Function
1	VDDRF1	Regulator Voltage for RF. A 220 nF capacitor should be placed between this pin and ground for regulator stability and noise rejection.
2	RBIAS	External bias resistor. A 36 kΩ resistor with 2% tolerance should be used.
3	CREGRF2	Regulator voltage for RF. A 220 nF capacitor should be placed between this pin and ground for regulator stability and noise rejection.
4	RFIO_1P	LNA positive Input in receive mode. PA Positive Output in transmit mode with differential PA.
5	RFIO_1N	LNA negative Input in receive mode. PA Negative Output in transmit mode with differential PA.
6	RFO2	Single-ended PA output
7	VDDBAT2	Power Supply pin two. Decoupling capacitors to the ground plane should be placed as close as possible to this pin.
8	NC	No Connect
9	CREGVCO	Regulator voltage for the VCO. A 220 nF capacitor should be placed between this pin and ground for regulator stability and noise rejection.
10	VCOGUARD	Guard/screen for VCO. This pin should be connected to Pin 9.
11	CREGSYNTH	Regulator voltage for the synthesizer. A 220 nF capacitor should be placed between this pin and ground for regulator stability and noise rejection.
12	CWAKEUP	External capacitor for wake-up control. A 150 nF capacitor should be placed between this pin and ground.
13	XOSC26P	The 26MHz reference crystal should be connected between this pin and XOSC26N.
14	XOSC26N	The 26MHz reference crystal should be connected between this pin and XOSC26P.
15	DGUARD	Internal guard/screen for the digital circuitry. A 220 nF capacitor should be placed between this pin and ground.
16	CREGDIG1	Regulator voltage for digital section of the chip. A 220 nF capacitor should be placed between this pin and ground for regulator stability and noise rejection.
17	GP0	Digital GPIO pin 0
18	GP1	Digital GPIO pin 1
19	GP2	Digital GPIO pin 2
20	IRQ_GP3	Interrupt Request, Digital GPIO test pin 3. An RC filter should be placed between this pin and the host microprocessor. Recommended values are R = 1.1 kΩ and C = 1.5 nF.
21	MISO	Serial port Master In Slave Out

22	SCLK	Serial port Clock
23	MOSI	Serial port Master Out Slave In
24	CSN	Chip select (active low). A pull-up to resistor of 100 kΩ, to VDD, is recommended to prevent the host microprocessor from inadvertently waking the ADF7023 from sleep.
25	GP4	Digital GPIO test pin 4
26	CREGDIG2	Regulator voltage for digital section of the chip. A 220 nF capacitor should be placed between this pin and ground for regulator stability and noise rejection.
27	XOSC32KP_GP5_ATB1	Digital GPIO test pin 5. A 32 kHz watch crystal can be connected between this pin and XOSC32KN_ATB2. Analog test pin 1.
28	XOSC32KN_ATB2	A 32 kHz watch crystal can be connected between this pin and XOSC32KP_GP5_ATB1. Analog test pin 2.
29	VDDBAT1	Digital Power Supply pin one. Decoupling capacitors to the ground plane should be placed as close as possible to this pin.
30	ADCIN_ATB3	Analog-to-Digital Converter Input. Analog test pin 3. Can be configured as an external PA enable signal.
31	ATB4	Analog test pin 4. Can be configured as an external LNA enable signal.
32	ADCVREF	ADC Reference output. A 220 nF capacitor should be placed between this pin and ground for adequate noise rejection.
EPAD	EPAD	Exposed package paddle. Connect to GND.

TYPICAL PERFORMANCE CHARACTERISTICS

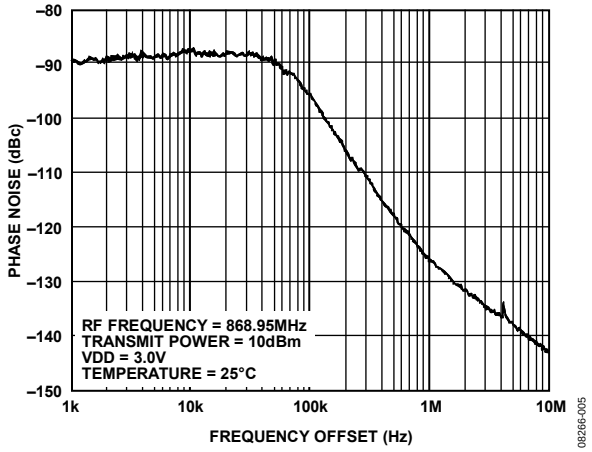


Figure 5. PLL Synthesizer Phase Noise Response at 868.95 MHz, Transmit Power = 10 dBm, V_{DD} = 3.0 V, T = 25°C

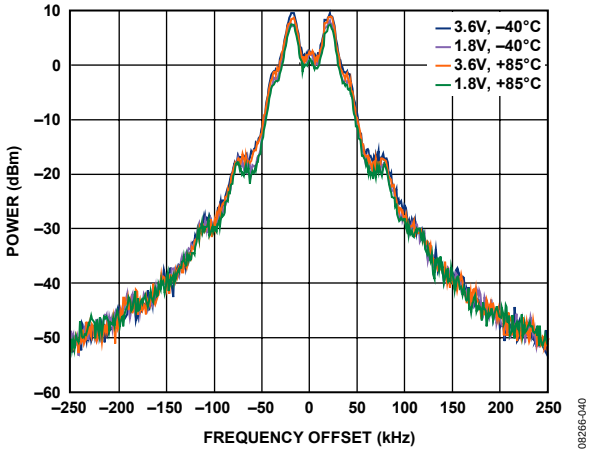


Figure 6. FSK Transmission Spectrum, f_{RF} = 868.95 MHz, f_{DEV} = 20 kHz, Data Rate = 38.4 kbps, PRBS9 Data

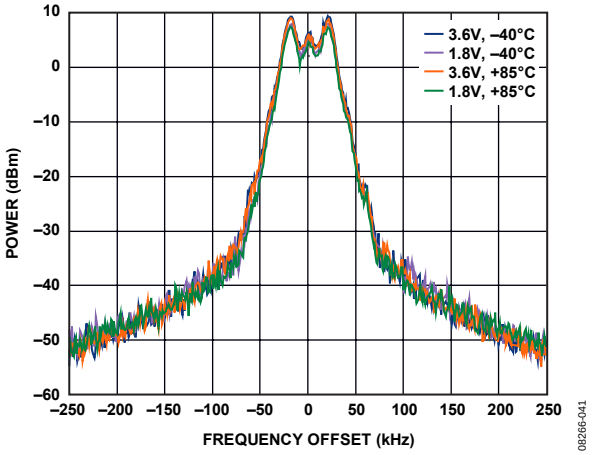


Figure 7. GFSK Transmission Spectrum, f_{RF} = 868.95 MHz, f_{DEV} = 20 kHz, Data Rate = 38.4 kbps, PRBS9 Data

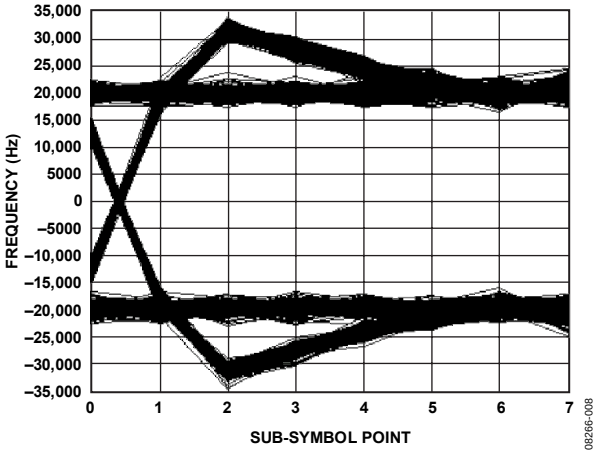


Figure 8. Tx Eye Diagram of Single-Ended PA (Overlay of 8000 Data Bits), Measured in a 1 MHz Bandwidth at Eight Samples Per Bit, FSK Modulation at 38.4 kbps with PRBS9 Data, and f_{DEV} = 20 kHz at 868.95 MHz, V_{DD} = 1.8 V, T = 25°C

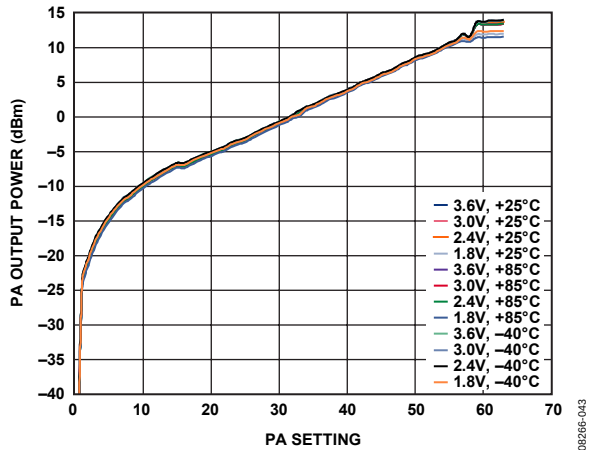


Figure 9. Single-Ended PA Output Power at 868.95 MHz vs. PA Level, Temperature, and V_{DD}

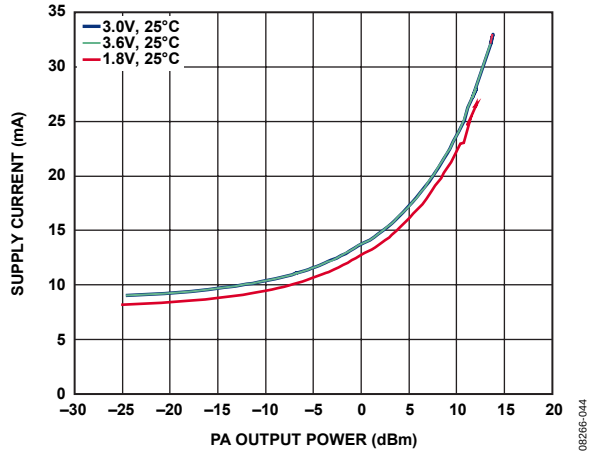


Figure 10. Supply Current of Single-Ended PA at 868.95 MHz vs. PA Output Power and V_{DD}

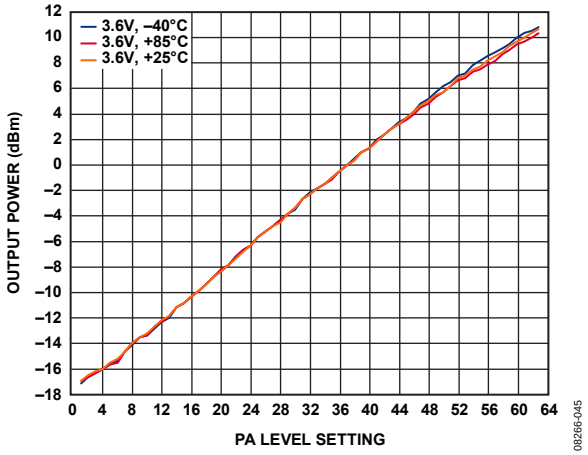


Figure 11. Differential PA Output Power at 868.95 MHz vs. PA Level and Temperature

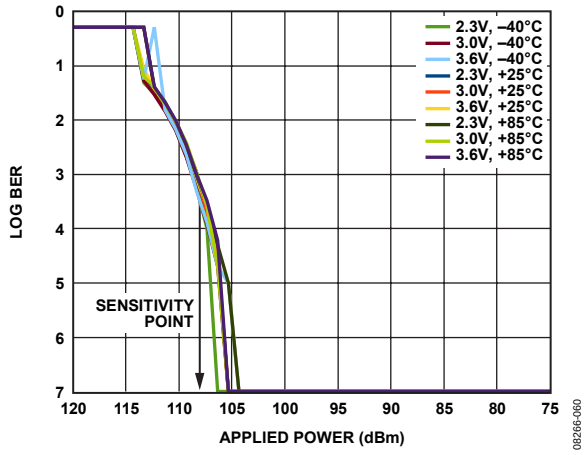


Figure 12. Bit Error Rate Sensitivity vs. V_{DD} and Temperature, f_{RF} = 868.95 MHz, Modulation = GFSK at 38.4 kbps, f_{DEV} = 20 kHz, V_{DD} = 3.0 V, T = 25°C

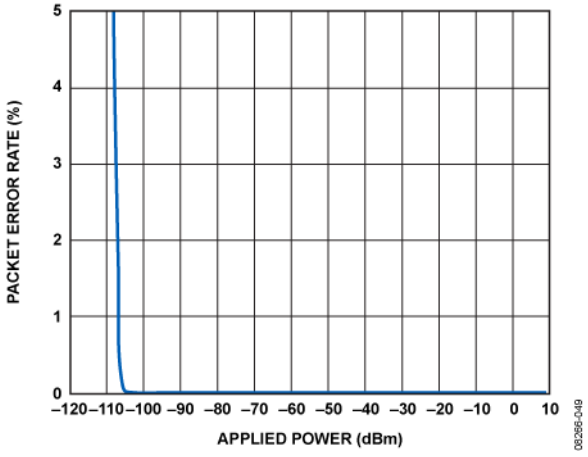


Figure 13. Packet Error Rate vs. RF input Level. 868MHz, GFSK, 38.4kbps, 20kHz Frequency Deviation, with 40-Bit Preamble per Data Point, V_{DD} = 3.0 V, T = 25°C

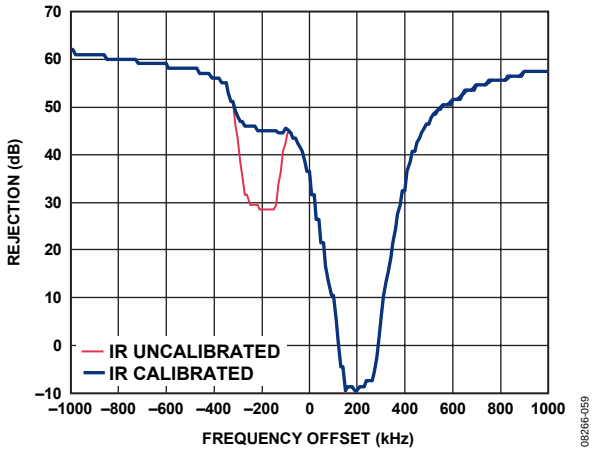


Figure 14. Receiver Blocking Performance to ±1 MHz Before and After Image Rejection Calibration, IF Filter Bandwidth = 100 kHz, f_{RF} = 868.95 MHz

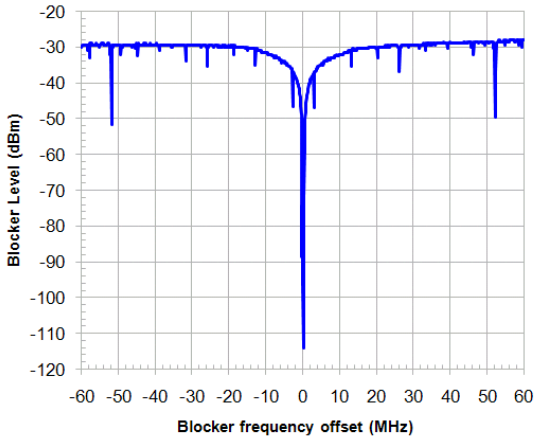


Figure 15. Wideband Receiver Blocking. f_{RF} = 868.95 MHz, Wanted signal: GFSK at 38.4 kbps, f_{DEV} = 20 kHz, V_{DD} = 3.0 V, T = 25°C, wanted signal level = sensitivity +3dB. Interferer signal: GFSK at 38.4 kbps, f_{DEV} = 20 kHz, V_{DD} = 3.0 V, T = 25°C

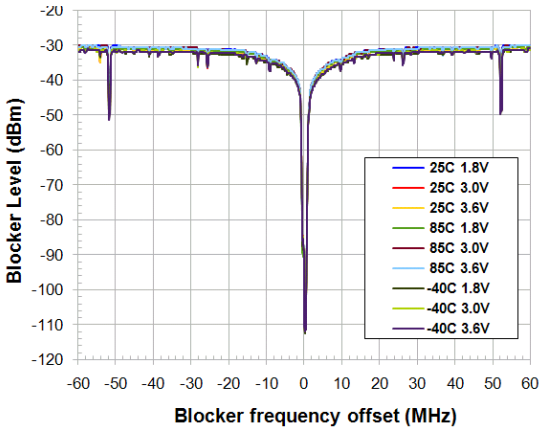


Figure 16. Wideband Receiver Blocking. f_{RF} = 915 MHz, Wanted signal: GFSK at 300 kbps, f_{DEV} = 75 kHz, wanted signal level = sensitivity +3dB. Interferer signal: GFSK at 300 kbps, f_{DEV} = 75kHz.

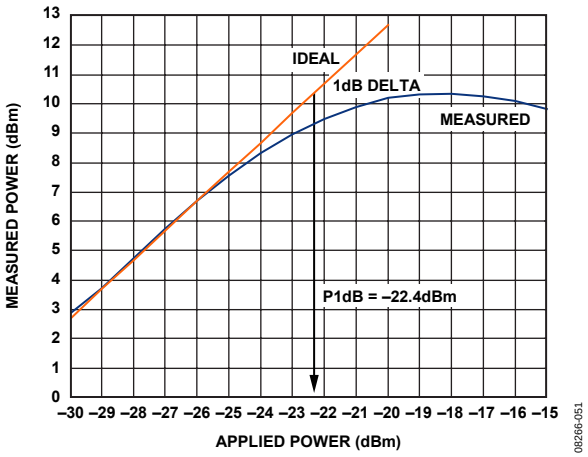


Figure 17. P1dB of Receiver at 868.95 MHz, at Maximum LNA and Mixer Gain, V_{DD} = 3.0 V, T = 25°C

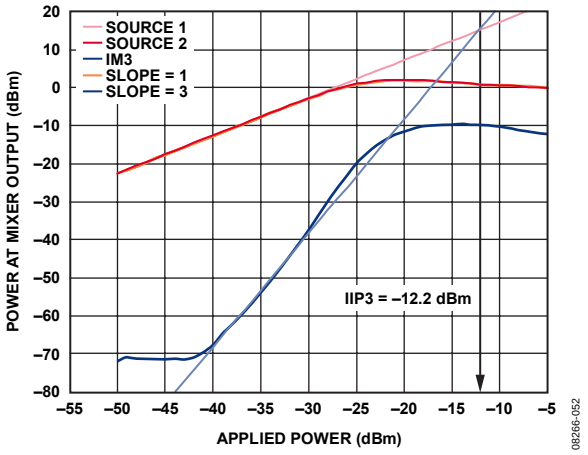


Figure 18. Third-Order Intermodulation Product, 868.95 MHz Channel at Maximum LNA and Mixer Gain, $f_{SOURCE1}$ = (868.95 + 1.1) MHz, $f_{SOURCE2}$ = (868.95 + 2.0) MHz, V_{DD} = 3.0 V, T = 25°C

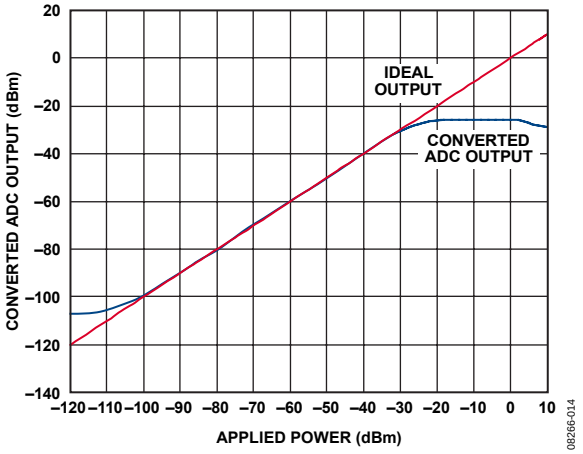


Figure 19. ADC Readback of RSSI vs. Applied Power Level, Readback Value Converted to dBm. Each Datapoint is an Average of 1000 Readbacks

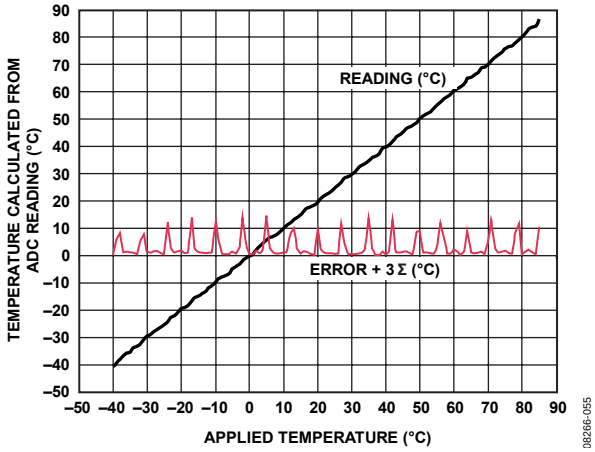


Figure 20. Average of 1000 Temperature Sensor Readbacks and 3 σ Error vs. Temperature, 3 σ Error Determined to be ±14°C, V_{DD} = 3 V, Average of 10 Readbacks Accurate to ±4.4°C

RADIO CONTROL

The ADF7023 has five radio states designated PHY_SLEEP, PHY_OFF, PHY_ON, PHY_RX and PHY_TX. The host microprocessor can transition the ADF7023 between states by issuing single byte commands over the SPI interface. The various commands and states are illustrated in Figure 21. The communications processor handles the enabling and disabling of various radio circuits and critical timing thereby simplifying radio operation and easing the burden on the host microprocessor.

RADIO STATES

PHY_SLEEP

In this state, the device is in a low power sleep mode. To enter the state the command CMD_PHY_SLEEP should be issued, either from the PHY_OFF or PHY_ON states. To exit the state the CSN pin can be set low, or the wake up controller (32.768kHz RC or 32.768kHz crystal) can be used to wake the radio from this state. The wake up timer should be setup before entering the PHY_SLEEP state. If retention of BBRAM contents is not required then Deep Sleep Mode 2 can be used to further reduce the PHY_SLEEP current consumption . Deep Sleep Mode 2 is entered by issuing the CMD_HW_RESET command. The options for PHY_SLEEP state are detailed in Table 9.

PHY_OFF

The 26 MHz crystal, the digital regulator and the synthesizer regulator are powered up. All memories are fully accessible. The BBRAM registers must be valid before exiting this state.

PHY_ON

Along with the crystal, the digital regulator and the synthesizer regulator, the VCO and RF regulators are powered up. A baseband filter calibration is performed when this state is entered from PHY_OFF if the bit bb_cal (mode_control, location 0x11A) is set. The device is ready to operate and the PHY_TX and PHY_RX states can be entered.

PHY_TX

The synthesizer is enabled and calibrated. The power amplifier is enabled and the device transmits at the channel frequency defined by the channel_freq[23:0] setting (0x109 to 0x10B). The state is entered by issuing the CMD_PHY_TX command.

The device automatically transmits the transmit packet stored in the packet RAM. After transmission of the packet, the PA is disabled and the device automatically returns to state PHY_ON and can optionally generate an interrupt.

In SPORT mode the device will transmit the data present on the GP2 pin as described in the SPORT section. The host microprocessor must issue the CMD_PHY_ON command to exit PHY_TX when in SPORT mode.

PHY_RX

The synthesizer is enabled and calibrated. The ADC, RSSI, IF filter, mixer and LNA are enabled. The radio is in receive mode on the current channel frequency.

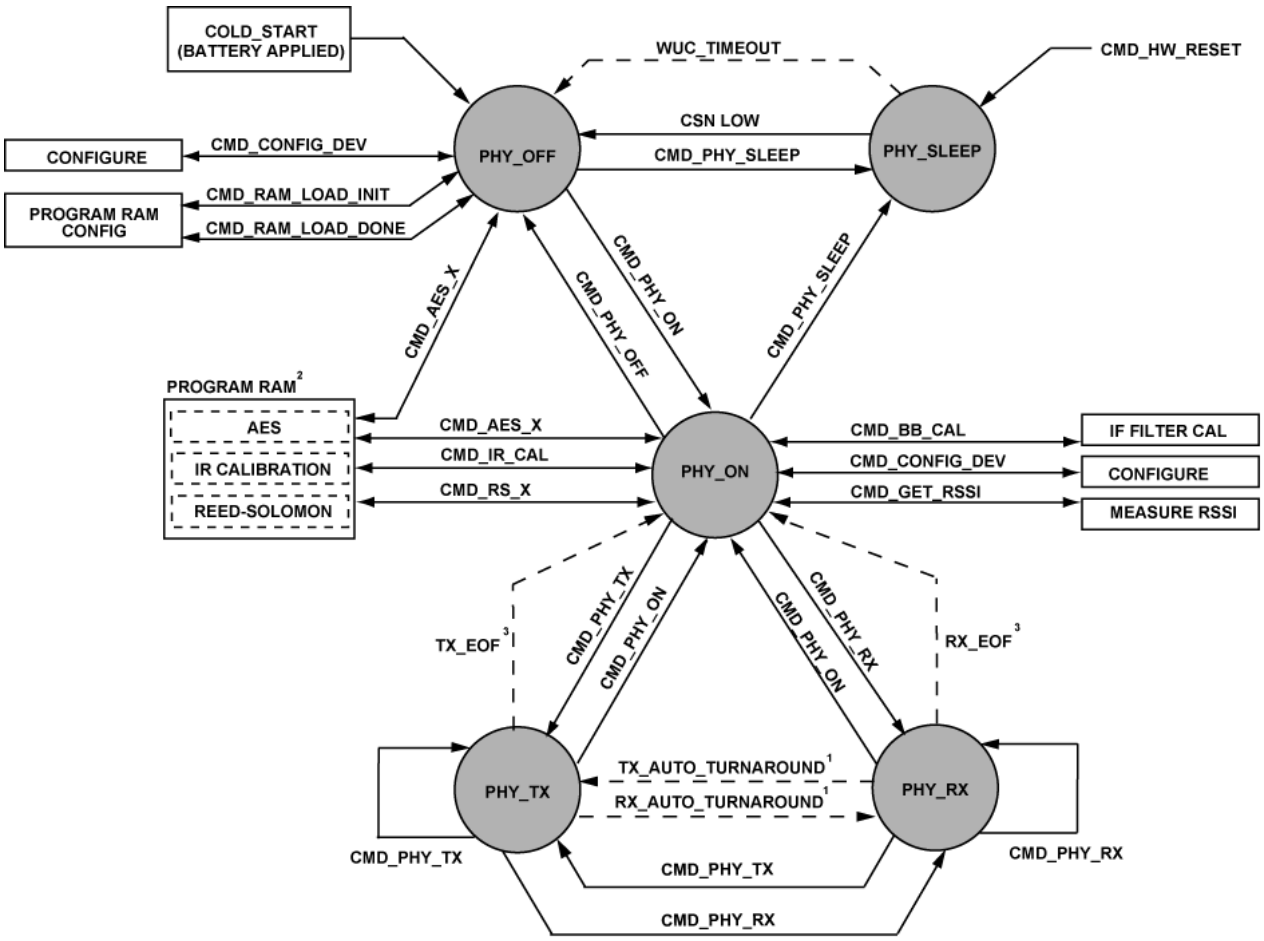
After reception of a valid packet, the device returns to the PHY_ON state and can optionally generate an interrupt. In SPORT mode the device remains in the PHY_RX state until the command CMD_PHY_ON is issued.

Current Consumption

The typical current consumption in the each state is detailed in Table 9.

Table 9. Current consumption in ADF7023 radio states

State	Current (typical)	Conditions
PHY_SLEEP (deep sleep mode 2)	0.15uA	Wake up timer off, BBRAM contents not retained. Entered by issuing CMD_HW_RESET
PHY_SLEEP (deep sleep mode 1)	0.3uA	Wake up timer off, BBRAM contents retained
PHY_SLEEP (RCO mode)	0.65uA	Wake up timer ON using 32kHz RC oscillator. BBRAM contents retained
PHY_SLEEP (XTOmode)	1.25uA	Wake up timer ON using 32kHz XTAL oscillator. BBRAM contents retained.
PHY_OFF	1.0mA	
PHY_ON	1.0mA	
PHY_TX	24.1mA	10dBm, single-ended PA, 868MHz
PHY_RX	12.8mA	



1. Transmit and receive automatic turnaround must be enabled by bits rx_auto_turnaround and tx_auto_turnaround (0x11A: mode_control)
2. AES encryption/decryption and image rejection calibration (IR cal) are only available if the necessary firmware module has been downloaded to the program RAM
3. The end of frame (EOF) automatic transitions are disabled in SPORT mode

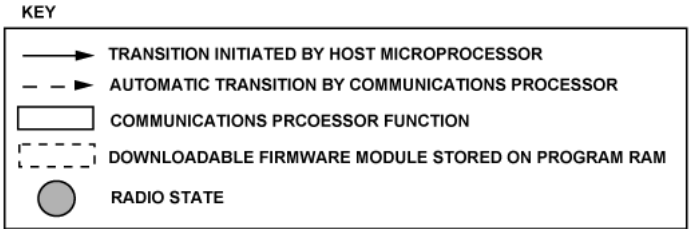


Figure 21. Radio State Diagram

INITIALISATION

After Application of Power

When power is applied to the ADF7023 ((VDDBAT1, VDDBAT2), it registers a power on reset event (POR) and transitions to the PHY_OFF state. The BBRAM memory is unknown, the packet RAM memory is cleared to 0x00 and the MCR memory is reset to its default values. The following procedure should be used by the host microprocessor:

- Bring the CSN line of the SPI low and wait until the MISO output goes high.
- Issue the CMD_SYNC command.
- Wait for the cmd_ready bit in the status word to go high.
- Configure the part by writing to all 64 of the BBRAM registers.
- Issue the command CMD_CONFIG_DEV so that the radio and packet handler settings are updated using the BBRAM values.
- The ADF7023 is now configured and ready to transition to PHY_ON.

After CMD_HW_RESET

The CMD_HW_RESET performs a full power down of all hardware and the device enters PHY_SLEEP. To complete the hardware reset the host microprocessor should follow the procedure detailed here:

- Wait for 1ms
- Bring the CSN line of the SPI low and wait until the MISO output goes high. The ADF7023 registers a POR and enters PHY_OFF.
- Issue the CMD_SYNC command.
- Wait for the cmd_ready bit in the status word to go high.
- Configure the part by writing to all 64 of the BBRAM registers.
- Issue the command CMD_CONFIG_DEV so that the radio and packet handler settings are updated using the BBRAM values.
- The ADF7023 is now configured and ready to transition to PHY_ON.

After CSN Low

The host microprocessor can bring CSN low at any time in order to wake the ADF7023 from the PHY_SLEEP state. This event is not registered as a POR event as the BBRAM contents are valid. The following is the procedure that the host microprocessor is required to follow:

- Bring the CSN line of the SPI low and wait until the MISO output goes high. The ADF7023 enters PHY_OFF.
- Issue the CMD_SYNC command.
- Wait for the cmd_ready bit in the status word to go high.
- Issue the command CMD_CONFIG_DEV so that the radio and packet handler settings are updated using the BBRAM values.
- The ADF7023 is now configured and ready to transition to PHY_ON.

After WUC timeout

The ADF7023 can autonomously wake from PHY_SLEEP using the wake-up controller. If the ADF7023 wakes after a WUC timeout in smart wake mode (SWM) it follows the SWM routine based on the smart wake mode configuration in BBRAM (see the Low Power Modes Section). If the ADF7023 wakes after a WUC timeout, with SWM disabled and the firmware timer disabled, it wakes in PHY_OFF and the following is the procedure that the host microprocessor is required to follow:

- Issue the CMD_SYNC command.
- Wait for the cmd_ready bit in the status word to go high.
- Issue the command CMD_CONFIG_DEV so that the radio and packet handler settings are updated using the BBRAM values.
- The ADF7023 is now configured and ready to transition to PHY_ON.

COMMANDS

The commands that are handled by the radio controller are detailed here. They initiate transitions between radio states or perform tasks as indicated in Figure 21.

CMD_PHY_OFF (0xB0)

This command transitions the ADF7023 to state PHY_OFF. It can be issued in PHY_ON. It powers down the RF and VCO regulators.

CMD_PHY_ON (0xB1)

This command transitions the ADF7023 to the PHY_ON state. If the command is issued in PHY_OFF it powers up the RF and VCO regulators and performs an IF filter calibration if the bb_cal bit is set in the mode_control register (0x11A). If the command is issued from PHY_TX state, the following procedure is performed by the communications processor:

- Ramp down the PA
- Set the external PA signal low (if enabled)
- Turn off the digital transmit clocks
- Power down the synthesizer
- Set fw_state = PHY_ON

If the command is issued from PHY_RX state, the following procedure is performed by the communications processor:

- Copy the measured RSSI to rssi_readback register
- Set the external LNA signal low (if enabled)
- Turn off the digital receiver clocks
- Power down the synthesizer and the receiver circuitry (ADC, RSSI, IF filter, mixer and LNA)
- Set fw_state = PHY_ON

CMD_PHY_SLEEP (0xBA)

This command transitions the ADF7023 to the very low power PHY_SLEEP state in which the WUC is operational (if enabled) and the BBRAM contents are retained.

CMD_PHY_RX (0xB2)

This command can be issued in the PHY_ON, PHY_RX or PHY_TX states. If the command is issued in the PHY_ON state, this is the procedure performed by the communications processor:

- Power up the synthesizer
- Power up the receiver circuitry (ADC, RSSI, IF filter, mixer and LNA)
- Set the RF channel
- Set the synthesizer bandwidth
- Do VCO calibration
- Delay for synthesizer settling
- Enable digital receiver blocks
- Set external LNA enable signal high (if enabled)
- Set fw_state = PHY_RX

If the command is issued in the PHY_RX state, this is the procedure performed by the communications processor:

- Set the external LNA signal low(if enabled)
- Unlock the AFC and AGC
- Turn off the receive clocks
- Set the RF channel
- Set the synthesizer bandwidth
- Do VCO calibration
- Delay for synthesizer settling
- Enable digital receiver blocks
- Set external LNA enable signal high (if enabled)
- Set fw_state = PHY_RX

If the command is issued in the PHY_TX state, this is the procedure performed by the communications processor:

- Ramp down the PA
- Set external PA signal low (if enabled)
- Turn off the digital transmit clocks
- Power up the receiver circuitry (ADC, RSSI, IF filter, mixer and LNA)
- Set the RF channel
- Set the synthesizer bandwidth
- Do VCO calibration
- Delay for synthesizer settling
- Enable digital receiver blocks
- Set external LNA enable signal high (if enabled)
- Set fw_state = PHY_RX

CMD_PHY_TX (0xB5)

This command can be issued in the PHY_ON, PHY_TX or PHY_RX states. If the command is issued in the PHY_ON state, this is the procedure performed by the communications processor:

- Power up the synthesizer
- Set the RF channel
- Set the synthesizer bandwidth
- Do VCO calibration
- Delay for synthesizer settling
- Enable digital transmit blocks
- Set the external PA enable signal high (if enabled)
- Ramp up the PA
- Set fw_state = PHY_TX
- Transmit data

If the command is issued in the PHY_TX state, this is the procedure performed by the communications processor:

- Ramp down the PA
- Set the external PA enable signal low (if enabled)
- Turn off digital transmit clocks
- Set the synthesizer bandwidth
- Do VCO calibration
- Delay for synthesizer settling
- Enable digital transmit blocks
- Set the external PA enable signal high (if enabled)
- Ramp up the PA
- Set fw_state = PHY_TX
- Transmit data

If the command is issued in the PHY_RX state, this is the procedure performed by the communications processor:

- Set the external LNA signal low(if enabled)
- Unlock the AFC and AGC
- Turn off the receive clocks
- Power down the receiver circuitry (ADC, RSSI, IF filter, mixer and LNA)
- Set the RF channel
- Set the synthesizer bandwidth
- Delay for synthesizer settling
- Enable digital transmit blocks
- Set the external PA enable signal high (if enabled)
- Ramp up the PA
- Set fw_state = PHY_TX
- Transmit data

CMD_CONFIG_DEV (0xBB)

This command interprets the BBRAM contents and sets up the radio parameters based on these contents. The user should setup the BBRAM contents and then issue the CMD_CONFIG_DEV. This command can be issued in the PHY_OFF or PHY_ON states.

CMD_GET_RSSI (0xBC)

This command turns on the receiver and performs an RSSI measurement on the current channel and then returns to the

ADF7023 to PHY_ON. The RSSI result is saved to the rssi_readback register (location 0x312). This command can only be issued from PHY_ON.

CMD_BB_CAL (0xBE)

This command performs an IF filter calibration. It can only be issued in the PHY_ON state. In many cases it may not be necessary to use this command as an IF filter calibration is automatically performed on the PHY_OFF to PHY_ON transition if bb_cal = 1 in register mode_control (location 0x11A).

CMD_SYNC (0xA2)

This command is used to allow the host microcontroller and communications processor to establish communications. After a application of power, WUC wakeup, CMD_HW_RESET or CMD_ RAM_LOAD_DONE the host should issue CMD_SYNC and wait until the cmd_ready status bit is high (refer to the Initialisation section). This process ensures that the next command issued by the host microprocessor will be processed by the communications processor.

CMD_HW_RESET (0xC8)

This command can be issued in any state and is independent of the state of the communications processor. The command performs a full power down of all hardware and the device enters PHY_SLEEP. To complete the hardware reset the CSN pin should be pulled low to wake the device from PHY_SLEEP. The procedure for initialisation of the device after CMD_HW_RESET is detailed in the Initialisation section.

CMD_RAM_LOAD_INIT (0xBF)

This command prepares the communications processor for a subsequent download of a software module to program RAM. This command should only be issued prior to the program RAM being written to by the host microprocessor.

CMD_RAM_LOAD_DONE (0xC7)

This command is only required after writing code to program RAM. It indicates to the communications processor that a software module has been loaded to program RAM. As the program RAM should only be written to in PHY_OFF the CMD_RAM_LOAD_DONE command can only be issued in PHY_OFF. The command will reset the communications processor and reset the packet RAM. This command should be followed by a CMD_SYNC.

CMD_IR_CAL(0xBD)

This command requires code to be uploaded to the ADF7023 RAM memory space. This code is available from ADI.

This command performs a fully automatic image rejection calibration on the ADF7023 receiver. The calibration results for quadrature phase correction and quadrature gain correction are returned to image_reject_cal_amplitude (0x119) and image_reject_cal_phase (0x118). For further information, refer to the Image Channel Rejection section.

CMD_AES_ENCRYPT (0xD0), CMD_AES_DECRYPT (0xD1) and CMD_AES_DECRYPT_INIT (0xD2)

These commands require the AES software module to be uploaded to the ADF7023 program RAM. The AES software module is available from ADI. Refer to the Downloadable Firmware Modules section for details on the AES encryption and decryption module.

AUTOMATIC STATE TRANSITIONS

On certain events the communications processor can automatically transition the ADF7023 between states. These automatic transitions are illustrated as dashed lines in Figure 21 and are explained here.

TX_EOF

The communications processor will automatically transition the device from PHY_TX to PHY_ON at the end of a packet transmission. On the transition the communications processor performs the following actions:

- Ramp down the PA
- Set the external PA signal low
- Disable the digital transmitter blocks
- Power down the synthesizer
- Set fw_state = PHY_ON

RX_EOF

The communications processor will automatically transition the device from PHY_RX to PHY_ON at the end of a packet reception. On the transition the communications processor performs the following actions:

- Copy the measured RSSI to rssi_readback register
- Set the external LNA signal low
- Disable the digital receiver blocks
- Power down the synthesizer and the receiver circuitry (ADC, RSSI, IF filter, mixer and LNA)
- Set fw_state = PHY_ON

TX_auto_turnaround

If the tx_auto_turnaround bit in the mode_control register (0x11A) is enabled then the device will automatically transition to PHY_TX at the end of a valid packet reception on the same RF channel frequency. On the transition the communications processor performs the following actions:

- Set the external LNA signal low
- Unlock the AGC and AFC (if enabled)
- Disable the digital receiver blocks
- Power down the receiver circuitry (ADC, RSSI, IF filter, mixer and LNA)
- Set RF channel frequency (same as previous receive)
- Enable the digital transmitter blocks
- Set the external PA signal high (if enabled)
- Ramp up the PA
- Set fw_state = PHY_TX
- Transmit data

In sport mode the TX_auto_turnaround transition is disabled.

RX_auto_turnaround

If the rx_auto_turnaround bit in the mode_control register (0x11A) is enabled then the device will automatically transition to PHY_RX at the end of a packet transmission, on the same RF channel frequency. On the transition the communications processor performs the following actions:

- Ramp down the PA
- Set the external PA signal low
- Disable the digital transmitter blocks
- Power up the receiver circuitry (ADC, RSSI, IF filter, mixer and LNA)
- Set RF channel frequency (same as previous transmit)
- Turn on AGC and AFC (if enabled)
- Enable the digital receiver blocks
- Set the external LNA signal high (if enabled)
- Set fw_state = PHY_RX

In sport mode the RX_auto_turnaround transition is disabled.

WUC timeout

The ADF7023 can use the WUC to wake from sleep on a timeout of the hardware timer. The device wakes into the PHY_OFF state. Refer to the WUC section for further details.

STATE TRANSITION AND COMMAND TIMING

The execution times for all radio state transitions are detailed in Table 10. Note that these times are typical and some can vary depending on the BBRAM configuration.

Table 10. ADF7023 command execution times

Description	Initiated by	Present State	Next State	Time (us), typical	Condition
CMD_HW_RESET	Host	any	PHY_SLEEP	TBD	
CMD_PHY_SLEEP	Host	PHY_OFF	PHY_SLEEP	TBD	
CMD_PHY_SLEEP	Host	PHY_ON	PHY_SLEEP	TBD	
CMD_PHY_OFF	Host	PHY_ON	PHY_OFF	226	
CMD_PHY_ON	Host	PHY_OFF	PHY_ON	261	including IF filter calibration
CMD_PHY_ON	Host	PHY_TX	PHY_ON	70	
CMD_PHY_ON	Host	PHY_RX	PHY_ON	70	
CMD_PHY_TX	Host	PHY_ON	PHY_TX	300	not including PA ramp up, including VCO calibration
CMD_PHY_TX	Host	PHY_RX	PHY_TX	300	including VCO calibration
CMD_PHY_TX	Host	PHY_TX	PHY_TX	300	not including PA ramp up/down, including VCO calibration
CMD_PHY_RX	Host	PHY_ON	PHY_RX	300	including VCO calibration
CMD_PHY_RX	Host	PHY_TX	PHY_RX	300	not including PA ramp up, including VCO calibration
CMD_PHY_RX	Host	PHY_RX	PHY_RX	300	including VCO calibration
CMD_GET_RSSI	Host	PHY_ON	PHY_ON	TBD	
CMD_CONFIG_DEV	Host	PHY_OFF	PHY_OFF	67	
CMD_CONFIG_DEV	Host	PHY_ON	PHY_ON	67	
CMD_BB_CAL	Host	PHY_ON	PHY_ON	144	
Tx_EOF	Automatic	PHY_TX	PHY_ON	70	not including PA ramp down
Rx_EOF	Automatic	PHY_RX	PHY_ON	70	
Tx_auto_turnaround	Automatic	PHY_RX	PHY_TX	TBD	no VCO calibration, not including PA ramp up
Rx_auto_turnaround	Automatic	PHY_TX	PHY_RX	TBD	no VCO calibration, not including PA ramp down
Warm start, WUC	Automatic	PHY_SLEEP	PHY_OFF	225	
Warm start, CSN low	Host	PHY_SLEEP	PHY_OFF	225	
Cold start	Application of Power	-	PHY_OFF	225	

PACKET MODE

The on-chip communications processor can be configured for use with a wide variety of packet based radio protocols using FSK/MSK /GFSK/GMSK /OOK modulation. The general packet format, when using the packet handling features of the communications processor, is illustrated Figure 22. To use the packet handling features the data_mode setting should be set to packet mode (location 0x126). 240 bytes of dedicated RAM (packet RAM) is available to store transmit and receive packets. In transmit mode preamble, sync word and CRC can be added by the communications processor to the data stored in the packet RAM for transmission. In addition, all packet data after the SWD can be optionally whitened, Manchester encoded or 8b/10b encoded on transmission and decoded on reception.

In receive mode the communications processor can be used to qualify received packets based on the preamble detection, sync word detection, CRC detection or address match and generate an interrupt on the IRQ_GP3 pin. On reception of valid packet the received payload data is loaded to packet RAM memory. Further information on interrupts is contained in the Interrupt Generation section.

Packet Structure	**PREAMBLE**	**SWD**	**PAYLOAD**			**CRC**	**POSTAMBLE**
Field			**Length**	**Address**	**Payload Data**		
Field length	1-256 bytes	1-24 bits	1 byte	1 – 9 bytes	0-240 bytes	2 bytes	2 bytes
Optional field							
Required only for variable packet length							
Comms processor adds in Tx, removed in Rx							
Host writes these fields to packet RAM							
Whitening/de-whitening (optional)							
Manchester encoding/decoding (optional)							
8b/10b encoding/decoding (optional)							
Fully programmable parameter		yes		yes	yes	yes	
Receive interrupt on valid field detection	yes	yes		yes		yes	
Programmable field error tolerance	yes	yes					
Programmable field offset (refer to Figure 26)			no	yes			

Figure 22. ADF7023 Packet Structure Description

PREAMBLE

This is a mandatory part of the packet that is automatically added by the communications processor when transmitting a packet and removed after receiving a packet. The preamble is a 0x55 sequence, with a programmable length between 1 and 256 bytes which is set in register preamble_len (0x11D). It is necessary to have preamble at the beginning of the packet to allow time for the receiver AGC, AFC and clock and data recovery circuitry to settle before the start of the sync word. The required preamble length will depend on the radio configuration. Refer to the Radio Blocks section for further details.

In receive mode the ADF7023 can use a preamble qualification circuit to detect preamble and interrupt the host microprocessor. The preamble qualification circuit tracks the received frame as a sliding window. The window is three bytes in length, and the preamble pattern is fixed at 0x55. The preamble bits are examined in "01"pairs. If either or both bits are in error, the pair is deemed erroneous. The possible erroneous pairs are "00", "11" and "10". The number of erroneous pairs tolerated in the preamble can be set using the preamble_match value according to Table 11.

Table 11. Preamble detection tolerance (preamble_match, location 0x11B)

Value	Description
0x0C	0 errors allowed
0x0B	1 erroneous bit-pair allowed in 12 bit-pairs
0x0A	2 erroneous bit-pairs allowed in 12 bit-pairs
0x09	3 erroneous bit-pairs allowed in 12 bit-pairs
0x08	4 erroneous bit-pairs allowed in 12 bit-pairs
0x00	Preamble detection disabled

If preamble_match is set to 0x0C the ADF7023 must receive 12 consecutive "01" pairs (3 bytes) to confirm valid preamble has been detected. The user can select the option to automatically lock the AFC and/or AGC at this point. The lock AFC on preamble detection can be enabled by setting afc_lock_mode = 0x3 (location 0x116: radio_cfg_10). The lock AGC on preamble detection can be enabled by setting agc_lock_mode = 0x3 (location 0x113: radio_cfg_7).

Once preamble has been detected the communications processor will search for sync word. From the end of preamble the communications processor will search for sync word for a duration equal to the sum of the number of programmed sync word bits, plus the preamble matching tolerance (in bits) plus 16 bits. This is illustrated in Figure 23. If sync word is detected during this duration the communications processor will load the received payload to packet RAM and compute the CRC (if enabled). If sync word is not detected during this duration the communications processor returns searching for preamble.

Preamble detection can be disabled by setting the preamble_match register to 0x00. To enable an interrupt upon preamble detection, the user must set interrupt_preamble_detect =1 (location 0x100: interrupt_mask_0).

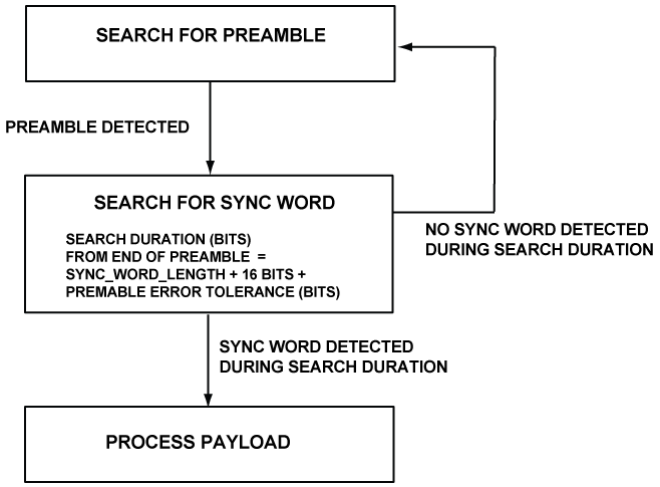


Figure 23. Search for preamble and search for sync word routine by the communications processor

SYNC WORD

This is the synchronization word and is used by the receiver for byte level synchronization, while also providing an optional interrupt on detection. It is automatically added to the packet by the communications processor in transmit and removed after receiving a packet.

The value of the SWD is set in registers sync_byte_0, sync_byte_1 and sync_byte_2 (locations 0x121, 0x122 and 0x123). The SWD is transmitted most significant bit first starting with sync_byte_0. The SWD matching length at the receiver is set using sync_word_length (0x120: sync_control) and can be 1 to 24 bits in length but the transmitted sync word is a multiple of 8 bits. Hence, for non-byte length sync words, the transmitted sync pattern should be appended with the preamble pattern as described in Figure 24 and Table 13.

In receive the ADF7023 can provide an interrupt on reception of the sync word sequence programmed in the sync_byte_0, sync_byte_1 and sync_byte_2 registers. This feature can be used to alert the host microprocessor that a valid packet has been received. An error tolerance parameter can also be programmed that accepts a valid match when up to three bits of the sync word sequence are incorrect. The error tolerance value is set using the sync_error_tol setting (location 0x120: sync_control) as described in Table 12.

Table 12. Sync word detection tolerance (sync_error_tol, location 0x120)

Value	Description
00	0 bit errors allowed
01	1 bit error allowed
10	2 bit errors allowed
11	3 bit errors allowed

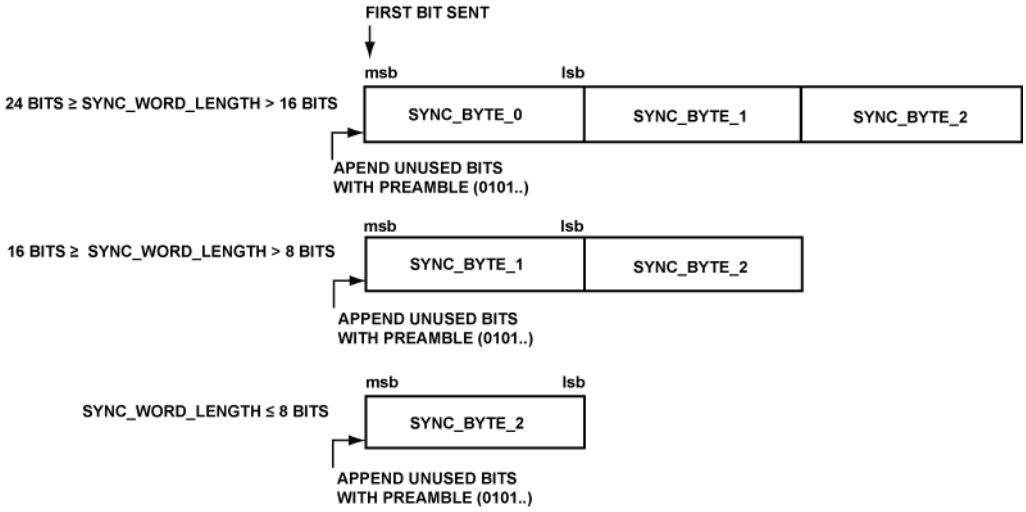


Figure 24. Transmit sync word configuration

Table 13. Sync word programming examples

Required sync word (binary, first bit being first in time)	sync_word_ length (0x120)	sync_ byte_0	sync_ byte_1	sync_ byte_2	Transmitted sync word (binary, first bit being first in time)	Receiver sync word match length (bits)
000100100011010001010110	24	0x12	0x34	0x56	0001_0010_0011_0100_0101_0110	24
111010011100101000100	21	0x5D	0x39	0x44	0101_1101_0011_1001_0100_0100	21
0001001000110100	16	0xXX	0x12	0x34	0001_0010_0011_0100	16
011100001110	12	0xXX	0x57	0x0E	0101_0111_0000_1110	12
00010010	8	0xXX	0xXX	0x12	0001_0010	8
011100	6	0xXX	0xXX	0x5C	0101_1100	6

PAYLOAD

This is the transmit data payload that the host microprocessor writes to the packet RAM. The location of transmit data in the packet RAM is defined by the tx_base_adr value (location 0x124) The tx_base_adr value is the location of the first byte of the transmit payload data in packet RAM. On reception of a valid sync word the communications processor automatically loads the receive payload to the packet RAM. The rx_base_adr value (location 0x125) sets the location in packet RAM of the first byte of the received payload. For more details on packet RAM memory, refer to the ADF7023 Memory Map section.

Byte Orientation

The over-the-air arrangement of each transmitted packet RAM byte can be set to MSB first or LSB first using the data_byte setting (location 0x126: packet_lenght_control). The same orientation setting should be used on the transmit and receive side of the RF link.

Packet Length Modes

The ADF7023 can be used in both fixed and variable length packet systems. Fixed or variable length packet mode is set using the packet_len variable (location 0x126: packet_length_control).

For a fixed packet length system the length of the transmit and received payload is set by the packet_length_max register (location 0x127). The payload length is defined as the number of bytes from the end of sync word to the start of the CRC.

In variable packet length mode the communications processor extracts the length field from the received payload data. The length field must be the first byte in the transmit payload.

The communications processor calculates the actual received payload length as:

$$Rx\ payload\ length = Length + length\_offset - 4$$

Where length is the length field (first byte in received payload) and length_offset (location 0x126: packet_length_control) is a programmable offset. The length_offset value is to allow compatibility with systems where the length field in the proprietary packet may also include the length of the CRC and/or the sync word. The ADF7023 defines the payload length as the number of bytes from the end of sync word to the start of the CRC. In variable packet length mode the packet_length_max value defines the transmit packet length and the maximum receivable packet length. This is described in Figure 25.

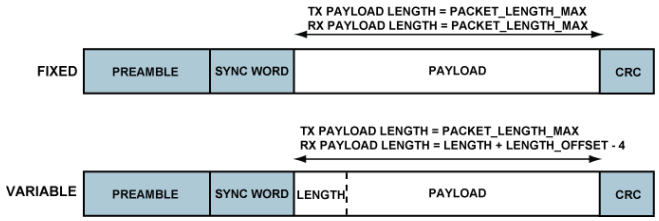


Figure 25. Payload length in fixed and variable length packet modes

Addressing

The ADF7023 provides a very flexible address matching scheme allowing matching of a single address, multiple addresses and broadcast addresses. The address information can be included at any section of the transmit payload. The location of the starting byte of the address data in the received payload is set by address_match_offset (location 0x129) as illustrated in Figure 26. The number of bytes in the address is set using address_length (location 0x12A). These settings allow the communications processor to extract the address information from the received packet. The address data is then compared against a list of known addresses which are stored in BBRAM (locations 0x12B to 0x13D). Each stored address byte has an associated mask byte thereby allowing matching of partial sections of the address bytes, which is useful for checking broadcast addresses or a family of addresses that have a unique identifier in the address sequence. The format and placement of the address information in the payload data should match the address check settings at the receiver to ensure exact address detection and qualification. Table 14 shows the register locations in the BBRAM that are used for setup of the address checking. If the address_length register is set to 0x00 then address checking is disabled.

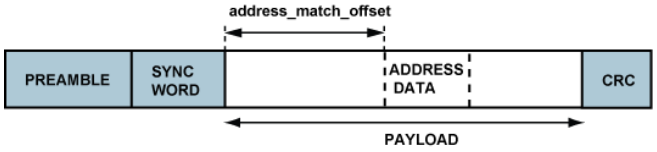


Figure 26. Address Match Offset

Table 14. Address Check Register Setup

Address (BBRAM)	Description
0x129: address_match_offset	Position of first address byte in received packet (first byte after SWD =0)
0x12A: address_length	Number of bytes in address field (N_{ADR})
0x12B	Address match byte 0
0x12C	Address mask byte 0
0x12D	Address match byte 1
0x12E	Address mask byte 1
:	:
	Address match byte N_{ADR}-1
	Address mask byte N_{ADR}-1
	0x00 to end or N_{ADR} for another address check sequence

The host microprocessor should set the interrupt_address_match bit if an interrupt is required on the IRG_GP3 pin. Further information on interrupts is contained in the Interrupt Generation section.

Example Address Check

Consider a system with 32-bit address lengths, in which the first byte is located in the 10th byte of the received payload data. The system also uses broadcast addresses in which the first byte is always 0xAA. To match the exact address, 0xABCDEF01 OR any broadcast address of the form 0xAAXXXXXX the ADF7023 must be configured as shown in Table 15.

Table 15. Example Address Check Configuration

BBRAM Address	Value	Description
0x129	0x09	Location in payload of 1st address byte
0x12A	0x04	N_{ADR}
0x12B	0xAB	Address Match Byte 0
0x12C	0xFF	Address Mask Byte 0
0x12D	0xCD	Address Match Byte 1
0x12E	0xFF	Address Mask Byte 1
0x12F	0xEF	Address Match Byte 2
0x130	0xFF	Address Mask Byte 2
0x131	0x01	Address Match Byte 3
0x132	0xFF	Address Mask Byte 3
0x133	0x04	N_{ADR} (to indicate another address check)
0x134	0xAA	Address Match Byte 0
0x135	0xFF	Address Mask Byte 0
0x136	0x00	Address Match Byte 1
0x137	0x00	Address Mask Byte 1
0x138	0x00	Address Match Byte 2
0x139	0x00	Address Mask Byte 2
0x13A	0x00	Address Match Byte 3
0x13B	0x00	Address Mask Byte 3
0x13C	0x00	End of addresses (indicated by 0x00)

CRC

An optional CRC-16 can be appended to the packet by setting crc_en =1 (0x126: packet_length_control). The default polynomial is used if prog_crc_en = 0 (symbol_mode, location 0x11C). The default CRC polynomial is:

$$g(x) = x^{16} + x^{12} + x^5 + 1$$

Any other 16-bit polynomial can be used if prog_crc_en = 1, and the polynomial is set in crc_poly_0 and crc_poly_1 (location 0x11E and 0x11F). The setup of the CRC is described in Table 16.

Table 16.CRC setup

crc_en (0x126)	prog_crc_en (0x11C)	Description
0	0	CRC disabled in transmit and CRC detection disabled in receive
0	1	CRC disabled in transmit and CRC detection disabled in receive
1	0	CRC enabled in transmit and CRC detection enabled in receive, with default CRC polynomial
1	1	CRC enabled in transmit and CRC detection enabled in receive, with CRC polynomial defined by

		crc_poly_0 and crc_poly_1

To convert a user defined polynomial to the two byte value, the polynomial should be written in binary format, with the x^{16} bit discarded. The remaining 16 bits then make up crc_poly_0 (most significant byte) and crc_poly_1 (least significant byte). Two examples of setting common 16-bit CRCs are shown in Table 17.

Table 17. Example: Programming of crc_poly_0 and crc_poly_1

Polynomial	Binary Format	crc_poly_0	crc_poly_1
$x^{16}+x^{15}+x^{2}+1$ (CRC-16-IBM)	1_1000_0000_0000_0101	0x80	0x05
$x^{16}+x^{13}+x^{12}+x^{11}+x^{10}+x^{8}+x^{6}+x^{5}+x^{2}+1$ (CRC-16-DNP)	1_0011_1101_0110_0101	0x3D	0x65

To enable CRC detection on the receiver, with the default CRC or user defined 16-bit CRC the crc_en (location 0x126: packet_length_control) should be set to 1. An interrupt on reception of a valid packet containing the correct CRC can be utilized by enabling the interrupt_crc_correct interrupt (interrupt_mask_0, location 0x100).

POST-AMBLE

The communications processor automatically appends 2 bytes of post-amble to the end of the transmitted packet. Each byte of post-amble is 0x55.The first byte is transmitted immediately after the CRC. The PA ramp down begins immediately after the first post_amble byte. The second byte is transmitted while the PA is ramping down.

On the receiver, if the received packet is valid, the RSSI is automatically measured during the first post-amble byte and the result stored in the rssi_readback register (location 0x312). The RSSI is measured by the communications processor 17us after the last CRC bit.

TRANSMIT PACKET TIMING

The PA ramp timing in relation to the transmit packet data is described in Figure 27. Once CMD_PHY_TX has been issued a VCO calibration is carried out followed by a delay for synthesizer settling. The PA ramp follows the synthesizer settling. After the PA has ramped up tpo the programmed rate there is 1 byte delay before the start of modulation (preamble). At the beginning of the second byte of post-amble the PA ramps down. The communications processor then transitions to the PHY_ON state or PHY_RX (if the tx_auto_turnaround bit is enabled or CMD_PHY_RX was issued).

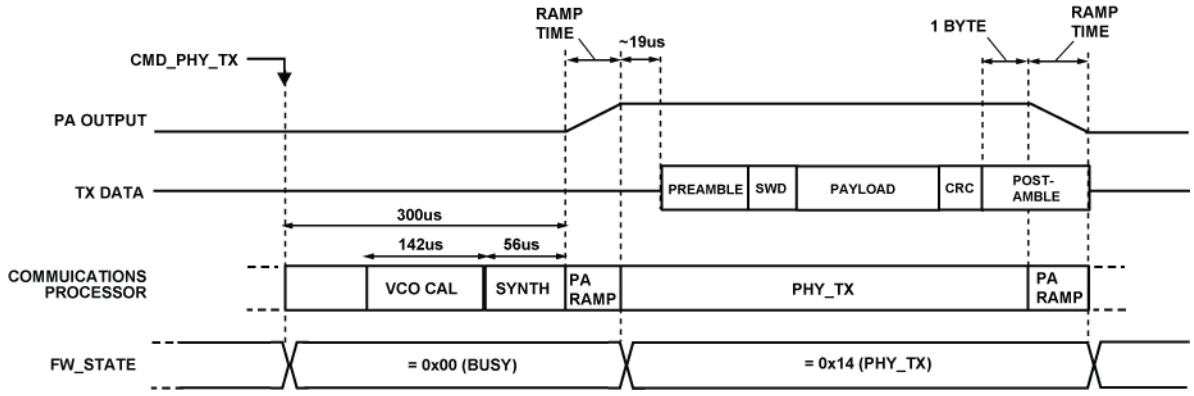


Figure 27. Transmit packet timing

DATA WHITENING

Data whitening can be employed to avoid long runs of ones or zeros in the transmitted data stream. This ensures sufficient bit transitions in the packet, which aids in receiver clock and data recovery as the encoding breaks up long runs of ones or zeros in the transmit packet. The data, excluding preamble and sync word, is automatically whitened before transmission by XOR-ing the data with an 8- bit pseudo-random sequence. At the receiver, the data is XOR-ed with the same pseudo-random sequence, thereby reversing the whitening. The linear feedback shift register polynomial used is X^7+X^1+1. Data whitening and de-whitening is enabled by setting data_whitening = 1 (location 0x11C: symbol_mode).

MANCHESTER ENCODING

Manchester encoding can be utilized to ensure a DC-free transmission. The encoded over-the-air bit rate (chip rate) will be double the rate set by the data_rate variable (locations 0x10C and 0x10D). A binary zero is mapped to "10" and a binary one is mapped to "01". The Manchester encoding and decoding is applied to the payload data and the CRC. Manchester Encoding must be employed for OOK modulation. Manchester encoding and decoding is enabled by setting manchester_enc =1 (location 0x11C: symbol_mode).

8B/10B ENCODING

8b/10b encoding is a byte orientated encoding scheme that maps an 8-bit byte to a 10-bit data block. It ensures the

maximum number of consecutive ones or zeros (i.e. run length) in any 10 bit transmitted symbol is 5. The advantage of this encoding scheme is that DC balancing is employed without the efficiency loss of Manchester encoding. The rate loss for Manchester encoding is 0.5 while for 8b/10b encoding the rate loss is 0.8. Encoding and decoding is applied to the payload data and the CRC. The 8b/10b encoding and decoding is enabled by setting eight_ten_enc =1 (location 0x11C: symbol_mode).

SPORT MODE

It is possible to bypass all of the packet handling features of the ADF7023 and use the SPORT interface for transmit and receive data. The SPORT interface is a high speed synchronous serial interface allowing direct interfacing to microcontrollers and DSPs. SPORT mode is enabled using the data_mode setting (location 0x126: packet_length_control) as described in Table 18. The SPORT mode interface is on the GPIO pins (GP0, GP1, GP2, GP4 and GP5). These GPIO pins can be configured using the gpio_configure setting (location 0x3FA) as described in Table 19.

SPORT mode provides a receive interrupt source on GP4. This interrupt source can be configured to provide an interrupt, or strobe signal, on either preamble detection or sync word detection. The type of interrupt is configured using the gpio_configure setting.

PACKET STRUCTURE IN SPORT MODE

In SPORT mode the host microprocessor has full control over the packet structure. However, the preamble frame is still required to allow sufficient bits for receiver settling (AGC, AFC and CDR). In SPORT mode sync word detection is not mandatory in the ADF7023, but can be enabled to provide byte level synchronization for the host microprocessor via the sync word detect interrupt or strobe on GP4. The general format of a SPORT mode packet is shown in Figure 28.

Figure 28. General SPORT mode packet

SPORT MODE IN TRANSMIT

Figure 29 illustrates the operation of the SPORT interface in transmit. Once in PHY_TX and with SPORT mode enabled, the data input of the transmitter is fully controlled by the SPORT interface (pin GP1). The transmit clock appears on GP2 pin. The transmit data from the host microprocessor should be synchronized with this clock. The fw_state variable in the status word or the cmd_finished interrupt can be used to indicate when the ADF7023 has reached the PHY_TX state and therefore is ready to begin transmitting data. The ADF7023 keeps transmitting the serial data presented at the GP1 input until the host microprocessor issues a command to exit the PHY_TX state.

SPORT MODE IN RECEIVE

The SPORT interface supports receive operation with a number of modes to suit particular signaling requirements. The receive data appears on the GP0 pin while the receive synchronized clock appears on the GP1 pin. The GP4 pin provides an interrupt or strobe signal on either preamble or sync word detection as described in Table 18 and Table 19. Once enabled the interrupt signal and strobe signals will remain operational while in PHY_RX. The strobe signal gives a single high pulse of 1-bit duration every 8 bits. The strobe signal is most useful when used with sync word detection as it is synchronized to the sync word and strobes the first bit in every byte.

TRANSMIT BIT LATENCIES IN SPORT MODE

The transmit bit latency is the time from the sampling of a bit by the transmit data clock on GP2 to when that bit appears at the RF output. There is no transmit bit latency when using FSK/MSK modulation. The latency when using GFSK/GMSK modulation is two bits. It is important that the host microprocessor keeps the ADF7023 in PHY_TX for two bit periods after the last data bit is sampled by the data clock to account for this latency when using GMSK/GFSK modulation.

Table 18. SPORT Mode setup

data_mode (location 0x126)	Description	GPIO Configuration
data_mode = 0	Packet Mode enabled. Packet handling controlled by communications processor.	-
data_mode = 1	SPORT mode enabled. Rx data and Rx clock enabled in PHY_RX (gpio_configure = 0xA0, 0xA3, 0xA6) Rx clock enabled in PHY_RX and Rx data enabled on preamble detect (gpio_configure = 0xA1, 0xA2, 0xA4, 0xA5, 0xA7, 0xA8)	GP0: Rx Data GP1: Tx Data GP2: Tx/Rx Clock GP4: interrupt or strobe enabled on preamble detect (depends on gpio_configure) GP5: depends on gpio_configure
data_mode = 2	SPORT mode enabled. Rx data and Rx clock enabled in PHY_RX if gpio_configure = 0xA0, 0xA3, 0xA6	GP0: Rx Data GP1: Tx Data GP2: Tx/Rx Clock GP4: interrupt or strobe enabled on sync word detect (depends on gpio_configure)

	Rx clock enabled in PHY_RX and Rx data enabled on preamble detect if gpio_configure = 0xA1, 0xA2, 0xA4, 0xA5, 0xA7, 0xA8	GP5: depends on gpio_configure

Table 19. GPIO functionality in SPORT Mode

gpio_configure	GP0	GP1	GP2	GP4	GP5
0xA0	Rx Data	Tx Data	Tx/Rx Clock	not used	not used
0xA1	Rx Data	Tx Data	Tx/Rx Clock	Interrupt	not used
0xA2	Rx Data	Tx Data	Tx/Rx Clock	Strobe	not used
0xA3	Rx Data	Tx Data	Tx/Rx Clock	not used	32.768kHz XTAL input
0xA4	Rx Data	Tx Data	Tx/Rx Clock	Interrupt	32.768kHz XTAL input
0xA5	Rx Data	Tx Data	Tx/Rx Clock	Strobe	32.768kHz XTAL input
0xA6	Rx Data	Tx Data	Tx/Rx Clock	not used	ext_uc_clk output
0xA7	Rx Data	Tx Data	Tx/Rx Clock	Interrupt	ext_uc_clk output
0xA8	Rx Data	Tx Data	Tx/Rx Clock	Strobe	ext_uc_clk output

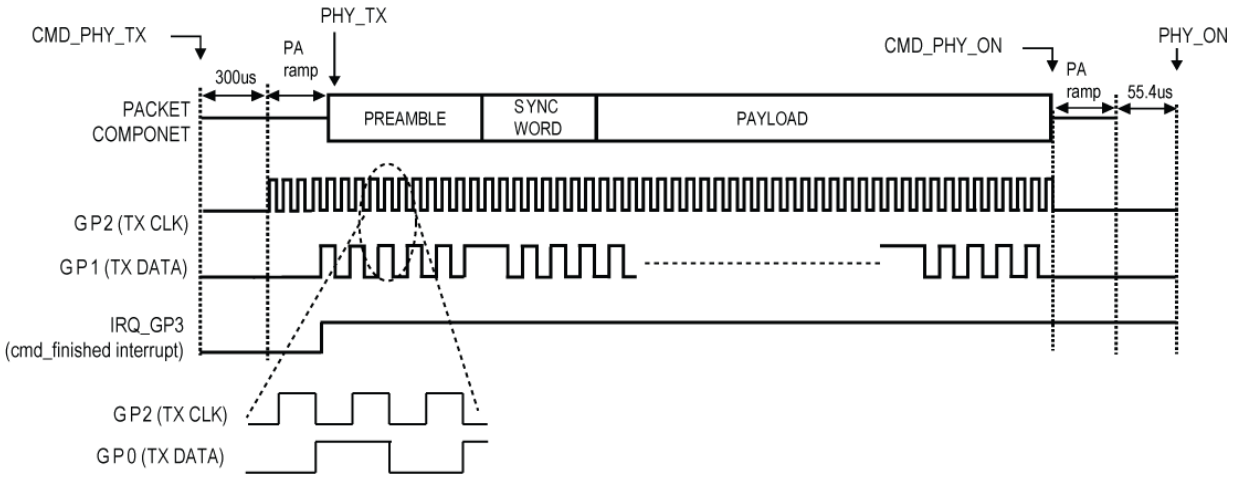


Figure 29. SPORT Mode transmit

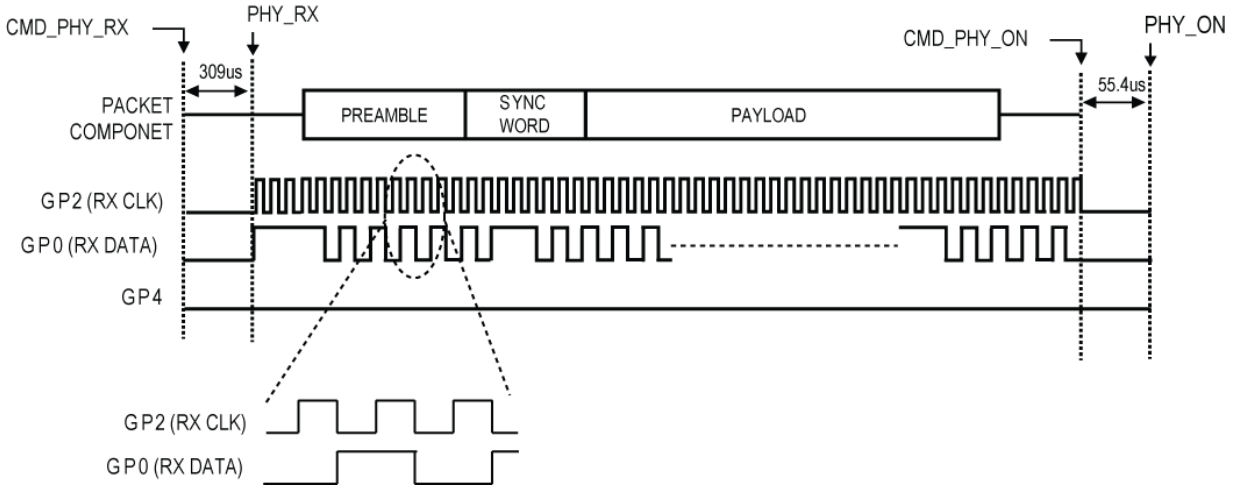


Figure 30. SPORT Mode receive, data_mode = 1, 2 and gpio_configure = 0xA0, 0XA3, 0xA6

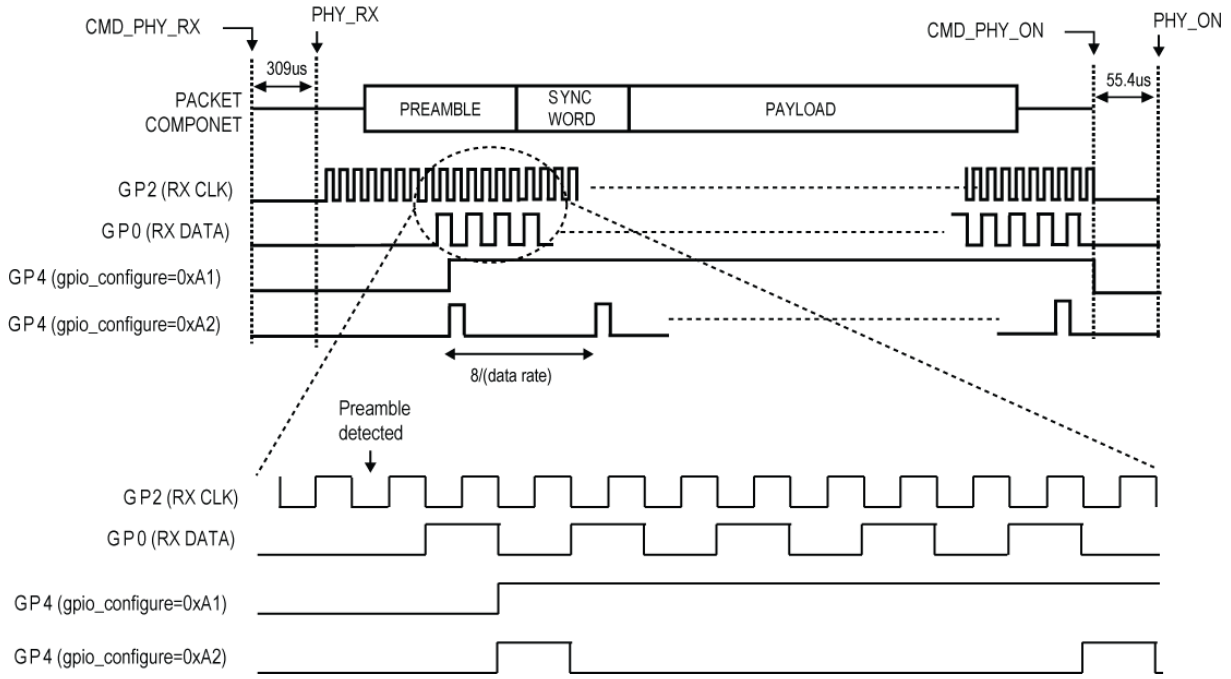


Figure 31. SPORT Mode receive, data_mode = 1, gpio_configure = 0xA1, 0xA2, 0xA4, 0xA5, 0xA7, 0xA8

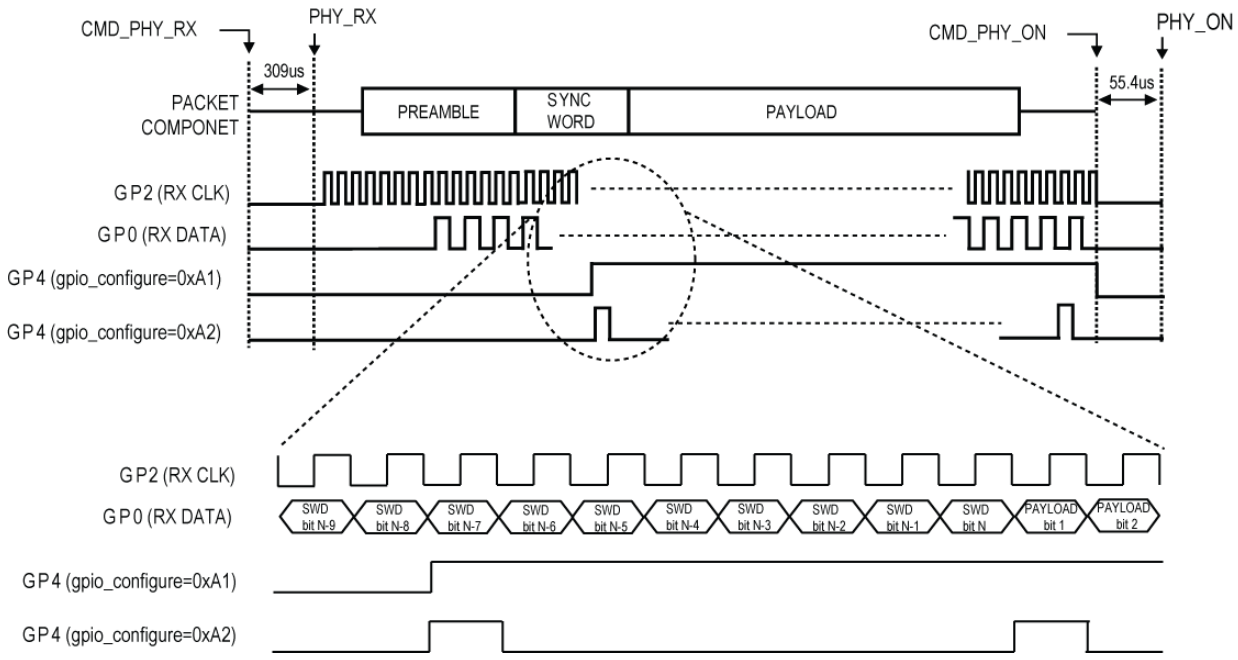


Figure 32. SPORT Mode receive, data_mode = 2, gpio_configure = 0xA1, 0xA2, 0xA4, 0xA5, 0xA7, 0xA8

INTERRUPT GENERATION

The ADF7023 utilises an efficient interrupt system comprising of MAC level Interrupts and PHY level interrupts. To enable an interrupt source the corresponding mask bit needs to be set. When an enabled interrupt occurs, the IRQ_GP3 pin will go high and the interrupt bit of the status word will be set to logic 1. The host microprocessor can either use the IRQ_GP3 pin or the status word to check for an interrupt. After an interrupt is asserted, the ADF7023 continues operations unaffected, unless it is directed to do otherwise by the host microprocessor. An outline of the interrupt source and mask system is shown in Table 20.

MAC interrupts can be enabled by writing a logic 1 to the relevant bits of interrupt_mask_0 (location 0x100) and PHY level interrupts, by writing a logic 1 to the relevant bits of interrupt_mask_1 (location 0x101). The structure of these memory locations is described in Table 20.

In the case of an interrupt condition, the interrupt source can be determined by reading the interrupt source registers interrupt_source_0 (location 0x336) and interrupt_source_1 (location 0x337). The bit that corresponds to the relevant interrupt condition will be high. The structure of these two registers is shown in Table 21.

Following an interrupt condition, the host microprocessor should clear the relevant interrupt flag, so that further interrupts will assert the IRQ_GP3 pin. This is performed by writing a logic 1 to the bit that is high in either the interrupt_source_0 or interrupt_source_1 registers. If multiple bits in the interrupt source registers are high, they can be cleared singly or altogether by writing logic 1s to them. The IRQ_GP3 pin will go low when all the interrupt source bits are cleared.

As an example, take the case where a battery_alarm interrupt has occurred. The host microprocessor should:

1. Read the interrupt source registers. In this example if none of the interrupt flags in interrupt_source_0 were enabled, only interrupt_source_1 needs to be read.
2. Clear the interrupt by writing 0x80h (or 0xFFh) to the interrupt_source_1.
3. Respond to the interrupt condition

Table 20. Structure of the interrupt mask registers

Register	Bit	Name	Interrupt Description
interrupt_mask_0 Address: 0x100	7	interrupt_num_wakeups	The number of WUC wakeups (number_of_wakeups[15:0]) has reached the threshold (number_of_wakeups_irq_threshold[15:0])
	6	interrupt_swm_rssi_det	RSSI above threshold interrupt (Smart Wake Mode)
	5	interrupt_aes_done	AES encryption/decryption complete interrupt
	4	interrupt_tx_eof	Packet transmission finished interrupt
	3	interrupt_address_match	Packet with address match interrupt
	2	interrupt_crc_correct	Packet with correct CRC interrupt
	1	interrupt_sync_detect	Sync word detection interrupt
	0	interrupt_preamble_detect	Preamble detection interrupt
interrupt_mask_1 Address: 0x101	7	battery_alarm	Battery voltage dropped below user set threshold value
	6	cmd_ready	Communications processor is ready to load a new command. Mirrors the cmd_ready bit of the status word
	5	unused	
	4	wuc_timeout	Wake up timer has timed out
	3	unused	
	2	unused	
	1	spi_ready	SPI ready for access
	0	cmd_finished	Communications processor is finished performing a command

Table 21. Structure of the interrupt source registers

Register	Bit	Name	Interrupt Description
interrupt_source_0 Address: 0x336	7	interrupt_num_wakeups	The number of WUC wakeups (number_of_wakeups[15:0]) has reached the threshold (number_of_wakeups_irq_threshold[15:0])
	6	interrupt_swm_rssi_det	RSSI above threshold interrupt (Smart Wake Mode)
	5	interrupt_aes_done	AES encryption/decryption complete interrupt
	4	interrupt_tx_eof	Packet transmission finished interrupt
	3	interrupt_address_match	Packet with address match interrupt
	2	interrupt_crc_correct	Packet with correct CRC interrupt
	1	interrupt_sync_detect	Sync word detection interrupt
	0	interrupt_preamble_detect	Preamble detection interrupt
interrupt_source_1 Address: 0x337	7	battery_alarm	Battery voltage dropped below user set threshold value
	6	cmd_ready	Communications processor is ready to load a new command. Mirrors the cmd_ready bit of the status word.
	5	unused	

	4	wuc_timeout	Wake up timer has timed out
	3	unused	
	2	unused	
	1	spi_ready	SPI ready for access
	0	cmd_finished	Communications processor is finished performing a command

INTERRUPTS IN SPORT MODE

In sport mode the interrupts from interrupt_source_1 are all available. However only interrupt_preamble_detect and interrupt_sync_detect are available from interrupt_source_0. A second interrupt pin is provided on GP4 which gives a dedicated SPORT mode interrupt on either preamble or sync word detection. For further details refer to the Sport Mode section

ADF7023 MEMORY MAP

This section describes the various memory locations used by the ADF7023. The radio control, packet management and smart wake mode capabilities of the part are realized through the use of an 8-bit, custom processor and an embedded ROM. The processor executes instructions stored in the embedded program ROM. There is also a local RAM, subdivided into three sections, that is used as a data packet buffer, both for transmitted and received data (packet RAM), and for storing the radio and packet handling configuration (BBRAM and MCR). The RAM addresses of these variables are 11 bits in length.

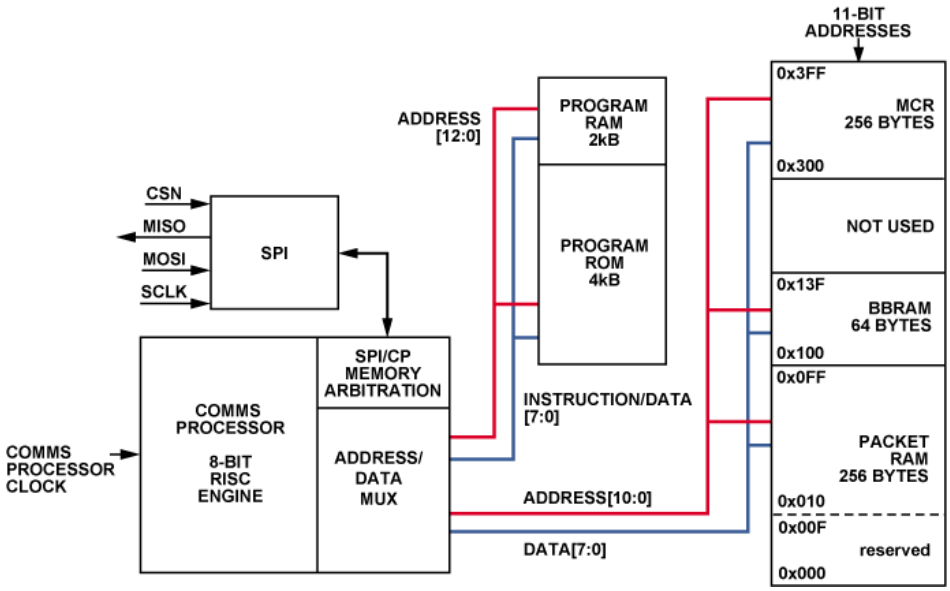


Figure 33. ADF7023 Memory Map

BBRAM

The battery backup RAM, or BBRAM, contains the main radio and packet handling registers used to configure the radio. On application of battery power to the ADF7023 for the first time the entire BBRAM should be initialized by the host microprocessor with the appropriate settings. Once the BBRAM has been written to the CMD_CONFIG_DEV should be issued to update the radio and communication processor with the current BBRAM settings. The CMD_CONFIG_DEVICE can only be issued in PHY_OFF or PHY_ON.

The BBRAM is used to maintain settings needed at wake-up from sleep mode by the wake-up controller. Upon wake-up from sleep, in smart wake mode, the BBRAM contents are read by the on-chip processor to recover the packet handling and radio parameters.

MODEM CONFIGURATION RAM(MCR)

The 256-byte modem configuration RAM, or MCR, contains the various registers used for direct control or observation of the physical layer radio blocks of the ADF7023. Contents of the MCR are not retained in the PHY_SLEEP state.

PROGRAM ROM

The program ROM consists of 4kbytes of non-volatile memory. It contains the firmware code for radio control, packet management and smart wake mode.

PROGRAM RAM

The program RAM consists of 2kbytes of volatile memory. This memory space is used for various software modules, such as AES encryption and IR calibration, which are available from ADI. The software modules are downloaded to the program RAM memory space over the SPI by the host microprocessor. Refer to the Memory Access section for details on how to write to the program RAM.

PACKET RAM

The Packet RAM consists of 256 bytes of memory space. The first 16 bytes of this memory space are allocated for use by the on-chip processor. The remaining 240 bytes of this memory is allocated for storage of data from valid received packets and packet data to be transmitted. The communications processor will store received payload data at the memory location indicated by the value of register rx_base_adr, the receive address pointer. The value of register tx_base_adr, the transmit address pointer, determines the start address of data to be transmitted by the communications processor. This memory can be arbitrarily assigned to store single or multiple transmit or receive packets both with and without overlap. The rx_base_adr value should be chosen to ensure that there is enough allocated packet RAM space for the maximum receiver payload length.

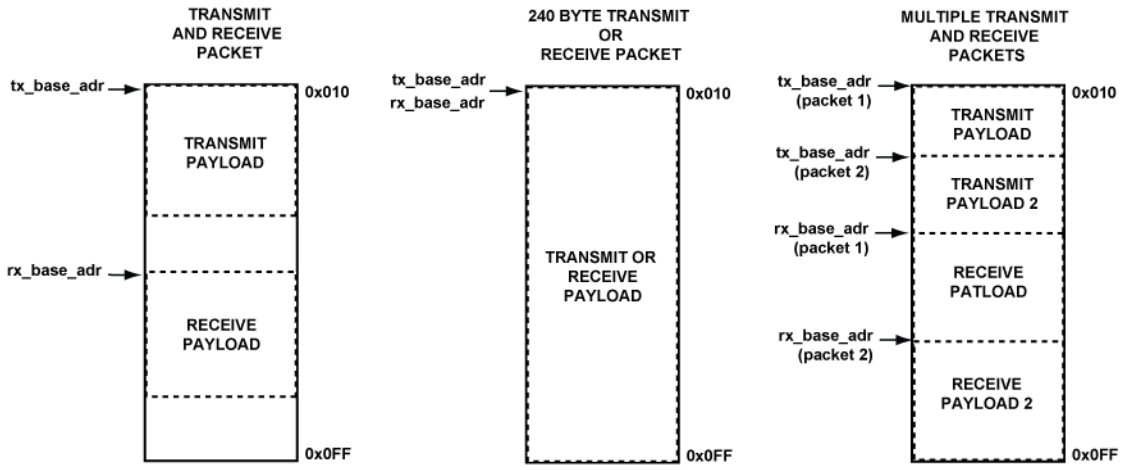


Figure 34. Example Packet RAM configurations using the tx packet and rx packet address pointers

SPI INTERFACE

GENERAL CHARACTERISTICS

The ADF7023 is equipped with a 4-wire SPI interface, using the SCLK, MISO, MOSI, and CSN pins. The ADF7023 always acts as a slave to the host microprocessor. Figure 35 shows an example connection diagram between the microprocessor and the ADF7023. The diagram also shows the direction of the signal flow for each pin. The SPI interface is active and the MISO output enabled only while the CSN input is low. The interface uses a word length of eight bits, which is compatible with the SPI hardware of most microprocessors. The data transfer through the SPI interface occurs with the most significant bit first. The MOSI input is sampled at the rising edge of SCLK. As commands or data are shifted in from the MOSI input at the SCLK rising edge, the status word or data is shifted out at the MISO pin synchronous with the SCLK clock falling edge. If CSN is brought low, the most significant bit of the status word appears on the MISO output without the need for a rising clock edge on the SCLK input.

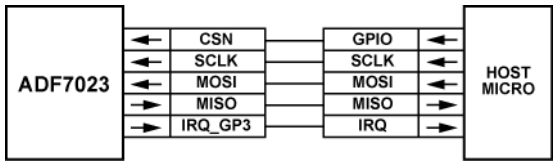


Figure 35. SPI interface Connections

COMMAND ACCESS

The ADF7023 is controlled through commands. Command words are single octet instructions that control the state transitions of the communications processor and access to the registers and packet RAM. The complete list of valid commands is given in the Command Reference section. Commands that have a CMD prefix are handled by the communications processor. Memory access commands have an SPI prefix and are handled by an independent controller. Thus, SPI commands can be issued independent of the state of the communications processor.

A command is initiated by bringing CSN low and shifting in the command word over the SPI a shown in Figure 36. All commands are executed after CSN goes high again or at the next positive edge of the SCLK input. The latter condition occurs in the case of a memory access command, in which case the command is executed on the positive SCLK clock edge corresponding to the most significant bit of the first parameter word. The CSN input must be brought high again after a command has been shifted into the ADF7023 to enable the recognition of successive command words. This is because a single command can only be issued during a CSN low period (with the exception of a double NOP command).

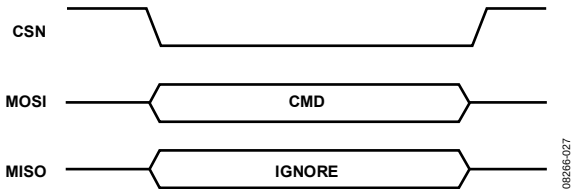


Figure 36. Command write (no parameters)

STATUS WORD

The status word of the ADF7023 is automatically returned over the MISO each time a byte is transferred over the MOSI. Shifting in double SPI_NOP commands, will cause the status word to be shifted out as shown in Figure 37. The meaning of the various bit fields is illustrated in Table 22. The fw_state variable can be used to read the current state of the communications processor and is described in

Table 23. If it is busy performing an action or state transition then fw_state will be busy. The fw_state variable also indicates the current state of the radio. The cmd_ready variable is used to indicate when the communications processor is ready to accept a new command. The status word should be polled and the cmd_ready bit examined before issuing a command to ensure that the communications processor is ready to accept a new command. It is not necessary to check the cmd_ready bit before issuing a SPI memory access command. It is possible to queue one command while the communications processor is busy. This is discussed in the Command Queuing section.

The ADF7023 interrupt handler can be also be configured to generate an interrupt signal on IRQ_GP3 when the communications processor is ready to accept a new command (cmd_ready interrupt, location 0x337: interrupt source_1) or when it has finished processing a command (cmd_finished interrupt, location 0x337: interrupt source_1).

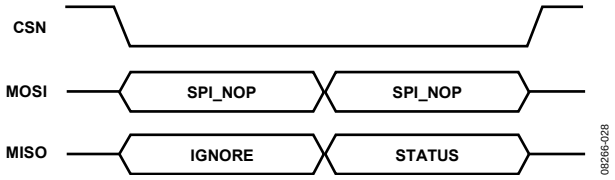


Figure 37. Reading the Status Word Using a Double SPI_NOP Command

Table 22. Status Word

Bit	Name	Description
[7]	spi_ready	0: SPI is not ready for access 1: SPI is ready for access
[6]	irq_status	0: no pending interrupt condition 1: pending interrupt condition (mirrors the IRQ_GP3 pin)
[5]	cmd_ready	0: the Radio Controller is not ready to receive a radio controller command 1: the Radio Controller is ready to receive a radio controller command
[4:0]	fw_state	Indicates the ADF7023 state (see Table 23)

Table 23. fw_state Description

Value	State
0x0F	Initializing
0x00	Busy. Performing a state transition
0x11	PHY_OFF
0x12	PHY_ON
0x13	PHY_RX
0x14	PHY_TX
0x06	PHY_SLEEP
0x05	Performing CMD_GET_RSSI
0x07	Performing CMD_IR_CAL
0x08	Performing CMD_AES_INIT
0x09	Performing CMD_AES_DEC
0x0A	Performing CMD_AES_ENC

COMMAND QUEUING

The cmd_ready status bit is used to indicate that the command queue used by the communications processor is empty. The queue is one command deep. The fw_state bit is used to indicate the state of the communications processor. The operation of the status word and these bits is illustrated in Figure 38 when a CMD_PHY_ON command is issued in PHY_OFF.

The operation of the status word when a command is being queued is illustrated in Figure 39, where a CMD_PHY_ON command is issued in state PHY_OFF followed quickly by a CMD_PHY_RX command. The CMD_PHY_RX command is issued while the fw_state is busy (i.e. transitioning between PHY_OFF and PHY_ON), but the cmd_ready bit is high indicating that the command queue is empty. Once the CMD_PHY_RX command has been issued the cmd_ready bit transitions to a logic low indicating the command queue is full. Once the PHY_OFF to PHY_ON transition is finished the PHY_RX command is processed immediately by the communications processor and the cmd_ready bit goes high, indicating that the command queue is empty and another command may be issued.

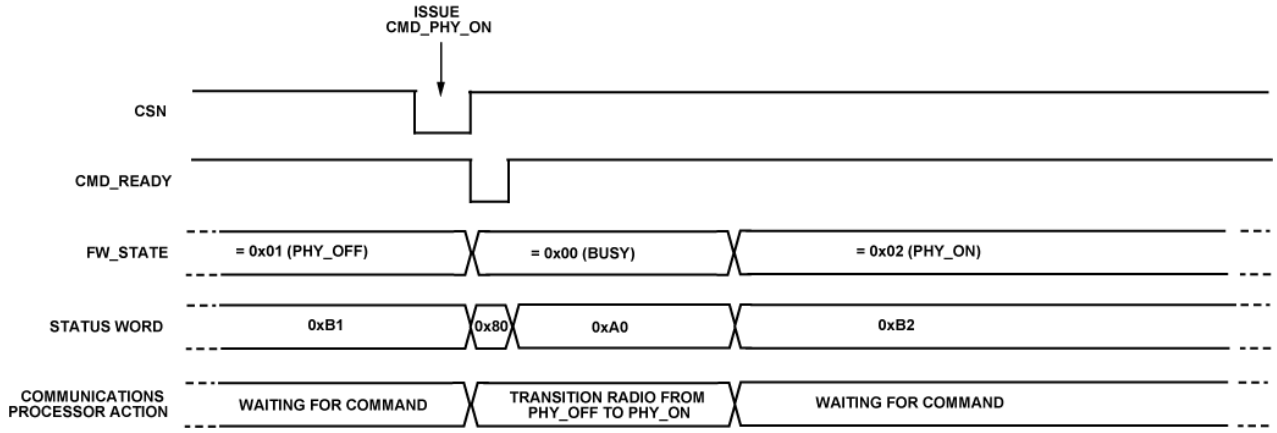


Figure 38. Operation of the cmd_ready and fw_state bits in transitioning the ADF7023 from PHY_OFF to PHY_ON

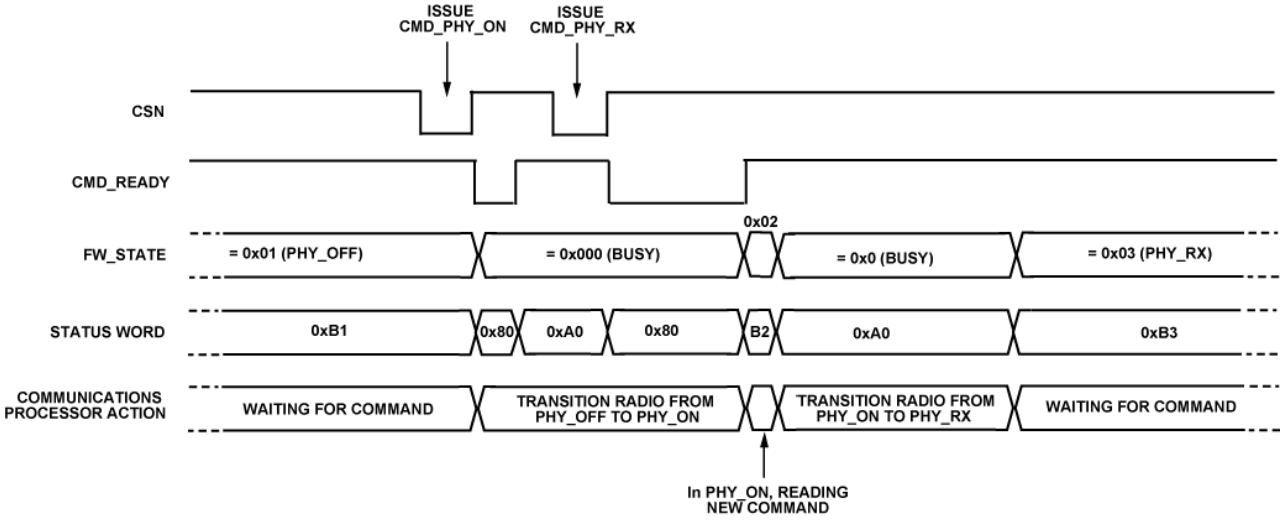


Figure 39. Command queuing and operation of the cmd_ready and fw_state bits in transitioning the ADF7023 from PHY_OFF to PHY_ON and then to PHY_RX

MEMORY ACCESS

Memory locations are accessed by invoking the relevant SPI command. An 11-bit address is used to identify registers or locations in the memory space. The most significant 3 bits of the address are incorporated into the SPI command by appending them as the lsbs of the command word. Figure 40 illustrates the command, address and data partitioning. The various SPI memory access commands are different depending on the memory location being accessed. This is described in Table 24.

An SPI command should only issued only if the spi_ready bit of the status word bit is high. The ADF7023 interrupt handler can be also be configured to generate an interrupt signal on IRQ_GP3 when the spi_ready bit is high (spi_ready, location 0x337: interrupt_source_1).

Also, an SPI command should not be issued while the communications processor is initializing (fw_state = 0x0F). SPI commands can be issued in any other communications processor state including the busy state (fw_state = 0x00). This allows the ADF7023 memory to be accessed while the radio is transitioning between states.

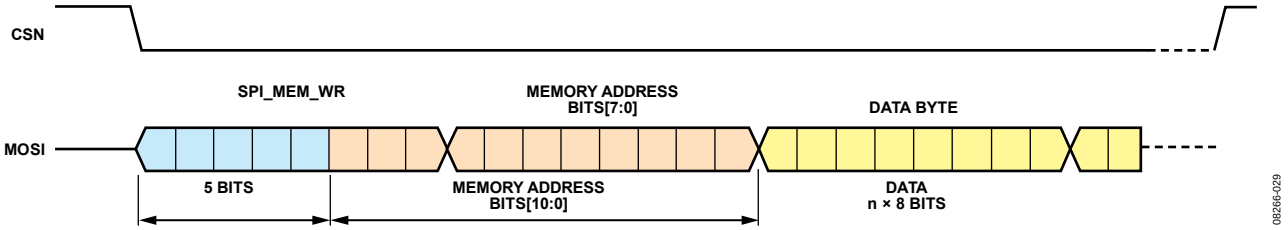


Figure 40.SPI Memory Access Command/Address Format

Table 24. Summary of SPI memory access commands

SPI Command	Command Value	Description
SPI_MEM_WR	= 0x18 (packet RAM) = 0x19 (BBRAM) = 0x1B (MCR) = 0x1A (program RAM)	Write data to BBRAM, MCR or packet RAM sequentially. An 11 bit address is used to identify memory locations. The most significant 3 bits of the address are incorporated in to the command (xxxb). This command is followed by the remaining 8 bits of the address.
SPI_MEM_RD	= 0x38 (packet RAM) = 0x39 (BBRAM) = 0x3B (MCR)	Read data from BBRAM, MCR or packet RAM sequentially. An 11 bit address is used to identify memory locations. The most significant 3 bits of the address are incorporated in to the command (xxxb). This command is followed by the remaining 8 bits of the address, which is subsequently followed by the appropriate number of SPI_NOP commands.
SPI_MEMR_WR	= 0x08 (packet RAM) = 0x09 (BBRAM) = 0x0B (MCR)	Write data to BBRAM/MCR or Packet RAM at random.
SPI_MEMR_RD	= 0x28 (packet RAM) = 0x29 (BBRAM) = 0x2B (MCR)	Read data from BBRAM/MCR or Packet RAM at random.
SPI_NOP	= 0xFF	No operation. Use for dummy writes when polling the status_word. Also used as dummy data on the MOSI line when performing a memory read.

Block Write

MCR, BBRAM and Packet RAM memory locations can be written to in block format using the SPI_MEM_WR command. The SPI_MEM_WR command code is 00011xxxb, where xxxb represent Bits[10:8] of the first 11-bit address. If more than one data byte is written, the write address is automatically incremented for every byte sent until CSN is set high which terminates the memory access command. Refer to Figure 41 for more details. The maximum block write for the MCR, packet RAM and BBRAM memories are 256 bytes, 256 bytes and 64 bytes respectively. These maximum block-write lengths should not be exceeded.

Example

Write 0x00 to the adc_config_high register (memory locations 0x35A).

- The first five bits of the SPI_MEM_WR command are 00011.
- The 11-bit address of ADC_Config_High is 01101011010.
- The first byte sent is 00011011 or 0x1B.
- The second byte sent is 01011010 or 0x5A.
- The third byte sent is 0x00.

Thus, 0x1B5A00 is written to the part.

Random Address Write

MCR, BBRAM and Packet RAM memory locations can be written to in random address format using the SPI_MEMR_WR

command. The SPI_MEMR_WR command code is 00001xxxb, where xxxb represent bits[10:8] of the 11-bit address. The lower 8 bits of the address should follow this command and then the data byte to be written to the address. The lower 8 bits of the next address are entered followed by the data for that address until all required addresses within that block are written, as shown in Figure 42.

Program RAM Write

The program RAM can only be written to using the memory block write as illustrated in Figure 41. The SPI_MEMR_WR should be set to 0x1A.

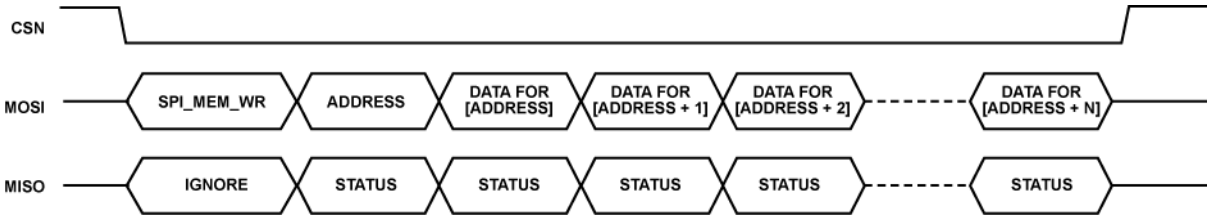


Figure 41. Memory(MCR, BBRAM or Packet RAM) Block Write

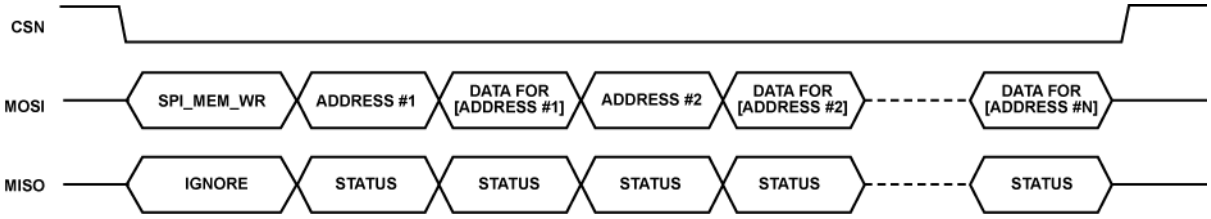


Figure 42. Memory (MCR, BBRAM or Packet RAM) Random Address Write

Block Read

MCR, BBRAM and Packet RAM memory locations can be read from in block format using the SPI_MEM_RD command. The SPI_MEM_RD command code is 00111xxxb, where xxxb represent Bits[10:8] of the first 11-bit address. This command is followed by the remaining 8 bits of the address to be read and then two SPI_NOP commands (dummy byte). The first byte available after writing the address should be ignored, with the second byte constituting valid data. If more than one data byte is to be read, the write address is automatically incremented for subsequent SPI_NOP commands sent. Refer to Figure 43 for more details.

Random Address Read

MCR, BBRAM and Packet RAM memory locations can be read from in a non-sequential manner using the SPI_MEMR_RD command. The SPI_MEMR_RD command code is 00101xxxb, where xxxb represent Bits[10:8] of the 11-bit address. This command is followed by the remaining 8 bits of the address to be written. Each subsequent address byte is then written. The last address byte to be written should be followed by two SPI_NOP commands as shown in Figure 44. The data bytes from memory, starting at the first address location are available after the second status byte.

Example

Read the value stored in the ADC_Config_High register.

- The first five bits of the SPI_MEM_RD command are 00111.
- The 11-bit address of ADC_Config_High is 01101011010.
- The first byte sent is 00111011 or 0x3B.
- The second byte sent is 01011010 or 0x5A.
- The third byte sent is 0xFF (SPI_NOP).
- The fourth byte sent is 0xFF.

Thus, 0x3B5AFFFF is written to the part.

The value shifted out on the MISO line while the 4th byte is sent is the value stored in the ADC_Config_High register.

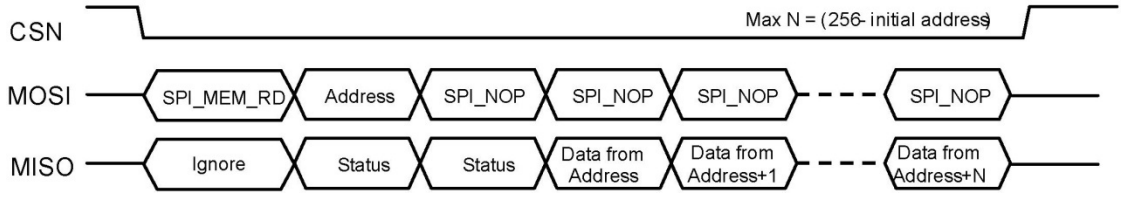


Figure 43. Memory(MCR, BBRAM or Packet RAM) Block Read

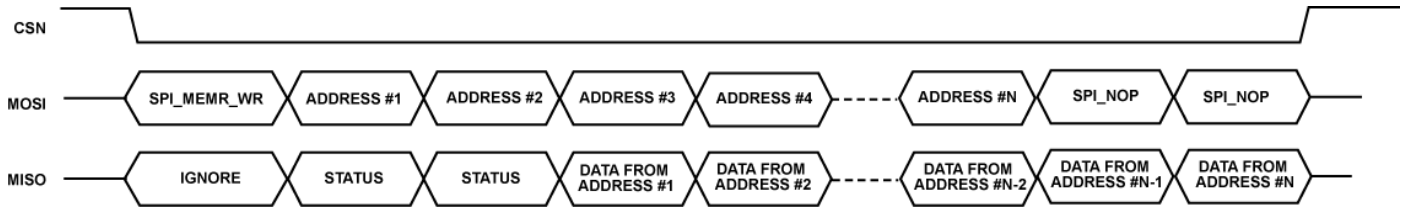


Figure 44. Memory (MCR, BBRAM or Packet RAM) Random Address Read

LOW POWER MODES

The ADF7023 has several low power modes to meet a wide variety of applications. These low powers modes are implemented using a hardware wake-up controller (WUC), a firmware timer and the smart wake mode functionality of the on-chip communications processor. The hardware WUC is a low power wake up controller (WUC) which comprises of a 16-bit wake-up timer with a programmable pre-scaler. The 32.768kHz RCOSC or XOSC provides the clock source for the timer.

The firmware timer is a software timer residing on the ADF7023. The firmware timer is used to count the number of WUC timeouts and so can be used to count the number of ADF7023 wakeups. The WUC and the firmware timer therefore provide a real-time clock capability.

Utilizing the low power WUC and the firmware timer, the SWM firmware allows the ADF7023 to wake up autonomously from sleep without intervention from the host microprocessor. During this wake-up period the ADF7023 is controlled by the communications processor. This functionality allows carrier sense, packet sniffing and packet reception while the host microprocessor is in sleep, thereby dramatically reducing overall system current consumption. The smart wake mode can then wake the host microprocessor on an interrupt condition. An overview of the low power mode configuration is shown in Figure 45 and the register settings that are used for the various low power modes are described in Table 25

Table 25. Settings for Low Power Modes

LPM	Memory Location	Register Name	Field	Description
Deep Sleep Modes	0x30D[1]	wuc_config_low	wuc_ bbram_en	Set to 0: BBRAM contents are not retained during PHY_SLEEP Set to 1: BBRAM contents are retained during PHY_SLEEP
WUC	0x30C[1]	wuc_config_high	wuc_prescaler[2:0]	Sets the pre-scaler value of the WUC
WUC	0x30D[1]	wuc_config_low	wuc _rcosc_en	Enables the 32.768kHz RC OSC
WUC	0x30D[1]	wuc_config_low	wuc_ xosc32k_en	Enables the 32.768kHz external OSC
WUC	0x30D[1]	wuc_config_low	wuc_ xosc32k_clksel	Sets the WUC clock source: 1:RC OSC selected 2: XOSC selected
WUC	0x30D[1]	wuc_config_low	wuc_arm	Enable to ensure device wakes from PHY_SLEEP on a WUC timeout
WUC	0x30E[2] 0x30F	wuc_value_high wuc_value_low	wuc_timer_value[15:0]	The WUC timer value. $\text{WUC interval (s)} = \frac{2^{(\text{wuc\_prescaler}+1)}}{32768}$
WUC	0x101	interrupt_mask_1	wuc_timeout	Enables the interrupt on WUC timeout
Firmware timer		interrupt_mask_0	interrupt_num_wakeups	Enabling this interrupt enables the firmware timer. Interrupt is set when the number_of wakeups count exceeds the threshold.
Firmware timer	0x102, 0x103	number_of_wakeups_0 number_of_wakeups_1	number_of_wakeups[15:0]	Number of ADF7023 wakeups.
Firmware timer	0x104, 0x105	number_of_wakeups_irq_threshold_0 number_of_wakeups_irq_threshold_1	number_of_wakeups_irq_threshold[15:0]	Threshold for the number of ADF7023 wakeups. When exceeded the ADF7023 will exit the low power mode.
SWM	0x11A	mode_control	swm_en	Enables Smart Wake Mode
SWM	0x11A	mode_control	swm_rssi_qual_en	Enables RSSI pre-qualification in smart wake mode
SWM	0x108	swm_rssi_thresh	swm_rssi_thresh[7:0]	RSSI threshold for RSSI pre-qualification. RSSI threshold (dBm) = swm_rssi_thresh -107
SWM	0x107	parmtime_divider	parmtime_divider[7:0]	Tick rate for the rx dwell timer.
SWM	0x106	rx_dwell_time	rx_dwell_time[7:0]	Time that ADF7023 remains awake during SWM. Receive dwell time (s) $= \text{rx\_dwell\_time} \times \frac{6.5MHz}{128 \times \text{parmtime\_divider}}$
SWM	0x100	interrupt_mask_0	interrupt_swm_rssi_det interrupt_preamble_detect interrupt_sync_detect interrupt_preamble_correct interrupt_address_match	Various interrupts that can be used in SWM

[1] It is necessary to write to both 0x30C and 0x30D registers in the following order: wuc_config_high (0x30C) directly followed by writing to wuc_config_low (0x30D).
[2] It is necessary to write to both 0x30E and 0x30F registers in the following order: wuc_value_high(0x30E) directly followed by writing to wuc_value_low (0x30F).

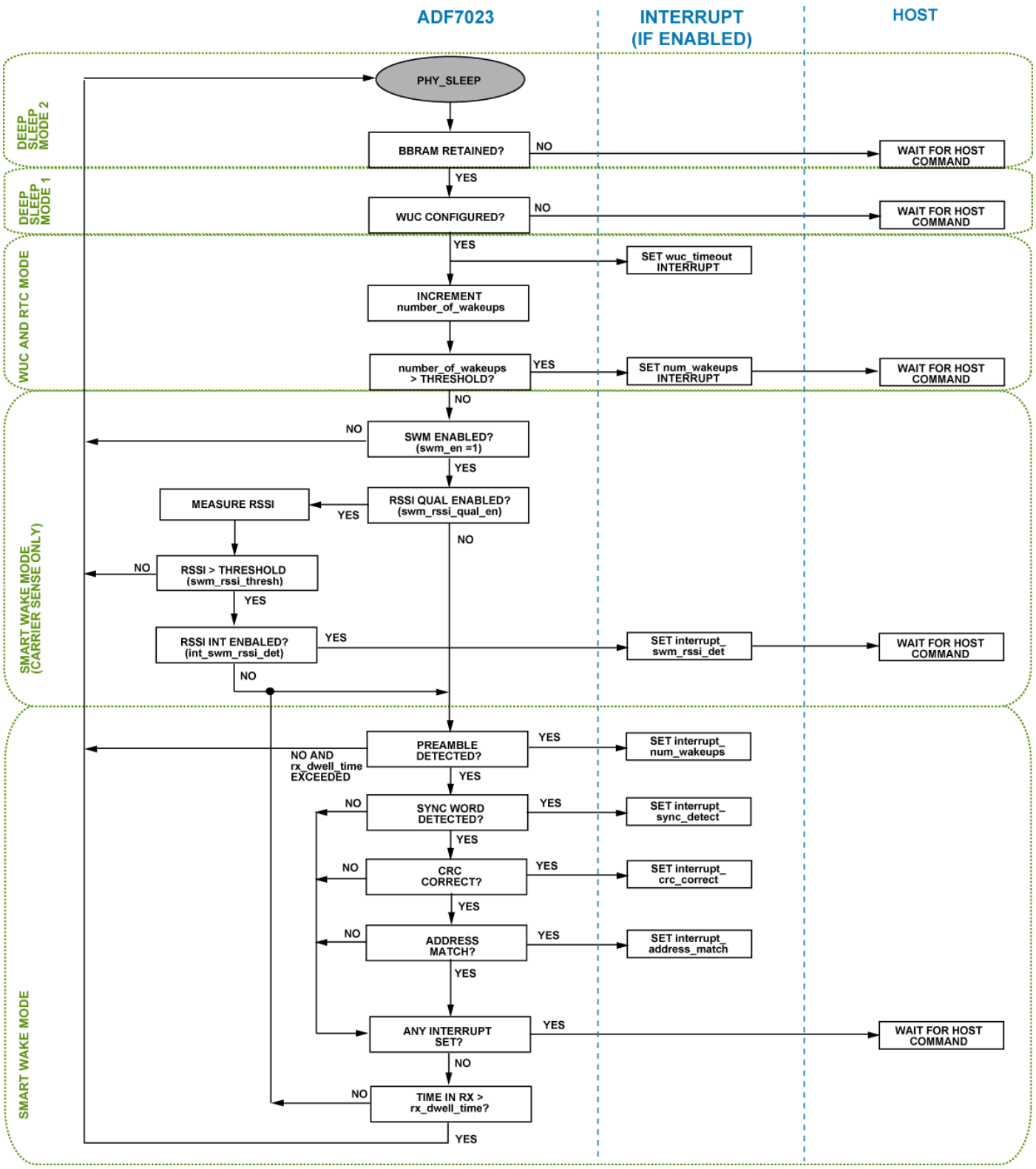


Figure 45. Low Power Mode Operation

EXAMPLE LOW POWER MODES

Deep Sleep Mode 2

This mode is suitable for applications where the host microprocessor is controlling the low power mode timing and where the lowest possible ADF7023 sleep current is required.

In this low power mode the ADF7023 is in PHY_SLEEP. The BBRAM contents are not retained. This low power mode is entered by issuing the CMD_HW_RESET command from any radio state. To wake the part from the PHY_SLEEP state the CSN pin should be set low. The initialization routine after a CMD_HW_RESET should be followed as detailed in the Radio Control section.

Deep Sleep Mode 1

This mode is suitable for applications where the host microprocessor is controlling the low power mode timing and where the ADF7023 configuration is retained during PHY_SLEEP.

In this low power mode the ADF7023 is in PHY_SLEEP with the BBRAM contents retained. Before entering the PHY_SLEEP state, wuc_config_low_bbram_en (location 0x30C) should be set to one to ensure that the BBRAM is retained. This low power mode is entered by issuing the CMD_PHY_SLEEP command from either the PHY_OFF or PHY_ON states. To exit the PHY_SLEEP state the CSN pin can be set low. The CSN low initialization routine should then be followed as detailed in the Radio Control section.

WUC Mode

In this low power mode the hardware WUC is used to wake the ADF7023 from the PHY_SLEEP state after a user-defined duration. At the end of this duration, the ADF7023 can provide an interrupt to the host microprocessor. While the ADF7023 is in the PHY_SLEEP state the host microprocessor can optionally be in a deep sleep state to save power.

Before issuing the CMD_PHY_SLEEP command, the host microprocessor should configure the WUC and set the firmware timer threshold to zero (number_of_wakeups_irq_threshold = 0). The wuc_config_low_bbram_en (location 0x30C) should be set to one to ensure that the BBRAM is retained. On issuing CMD_PHY_SLEEP the device then goes to sleep for a period until the hardware timer times out. At this point, the device wakes up, and if the wuc_interrupt or the interrupt_num_wakeups is enabled the device asserts the IRQ_GP3 pin.

The operation of this low power mode is illustrated in Figure 46.

WUC Mode with Firmware Timer

In this low power mode the WUC is used to periodically wake the ADF7023 from PHY_SLEEP and the firmware timer is used count the number of WUC timeouts. The combination of the WUC and the firmware timer provide a real-time clock (RTC) capability.

The host microprocessor should set up the WUC and the firmware timer before entering PHY_SLEEP. The wuc_config_low_bbram_en (location 0x30C) should be set to one to ensure that the BBRAM is retained. The WUC can be configured to timeout at some standard time interval (1s, 60s etc.). On issuing the CMD_PHY_SLEEP command, the device enters PHY_SLEEP for a period until the hardware timer times out. At this point, the device wakes up, increments the 16-bit firmware timer (number_of_wakeups) and if the wuc_interrupt is enabled the device asserts the IRQ_GP3 pin. If the16-bit firmware count is less than or equal to the user set value (number_of_wakeups_irq_threshold), the device returns to PHY_SLEEP. With this method, the firmware count (numer_of_wakeups) equates to a real time interval.

When the firmware count exceeds a threshold (number_of_wakeups_irq_threshold) the ADF7023 asserts the IRQ_GP3 pin, if the interrupt_num_wakeups bit is set and then enters PHY_OFF. The operation of this low power mode is illustrated in Figure 47.

Smart Wake Mode (Carrier Sense only)

In this low power mode the WUC, firmware timer and smart wake mode are used to implement periodic RSSI measurements on a particular channel (i.e. carrier sense). To enable this mode the WUC and firmware timer should be configured before entering PHY_SLEEP. The wuc_config_low_bbram_en (location 0x30C) should be set to one to ensure that the BBRAM is retained. The RSSI measurement is enabled by setting swm_rssi_qual = 1 (mode_control, location 0x11A) and setting swm_en = 1 (mode_control, location 0x11A). The interrupt_swm_rssi_det (interrupt _mask_0, location 0x100) should also be enabled. If the measured RSSI value is below the user defined threshold, swm_rssi_thresh (location 0x108), then the device will return to PHY_SLEEP. If the RSSI measurement is greater than the swm_rssi_thresh value, the device sets the interrupt_smw_rssi_det interrupt to alert the host microprocessor and waits in PHY_ON for a host command. The operation of this low power mode is illustrated in Figure 48.

Smart Wake Mode

In this low power mode the WUC, firmware timer and smart wake mode are employed to periodically listen for packets. To enable this mode the WUC and firmware timer should be configured and SMW enabled (swm_en location 0x11A), before entering PHY_SLEEP. The wuc_config_low_bbram_en (location 0x30C) should be set to one to ensure that the BBRAM is retained. The RSSI pre-qualification can be optionally enabled (swm_rssi_qual = 1). When RSSI pre-qualification is enabled the ADF7023 will only begin searching for preamble if the RSSI measurement is greater than the user-defined threshold.

The ADF7023 will be in PHY_RX for a duration determined by the rx_dwell_time setting (location 0x106). If the ADF7023 detects preamble during the receive dwell time it will then

search for sync word. If sync word is detected it will load the received data to packet RAM and check for a CRC and address match if enabled. If any of the receive packet interrupts have been set then the ADF7023 will return to PHY_ON and wait for a host command.

If the ADF7023 has received preamble detection during the receive dwell time but the remainder of the received packet extends beyond the dwell time then the ADF7023 will extend the dwell time until all of the packet has been received or the packet has been recognized as invalid (e.g. incorrect sync word).

This low power mode terminates when a valid packet interrupt has been received. Alternatively, this lower power can be terminated by using the firmware timer to count a certain number of ADF7023 wakeups or real-time interval. This can be useful if certain radio tasks (e.g. IR calibration) or microprocessor tasks need to be run periodically while in the low power mode.

The operation of this low power mode is illustrated in Figure 49.

Exiting low power mode

As described in Figure 45 the low power modes wait for a host command on termination. It is also possible to exit any of the low power modes, while the device is in PHY_SLEEP, by bringing CSN low and following the CSN low initialisation routine described in the Initialisation section.

LOW POWER MODE TIMING DIAGRAMS

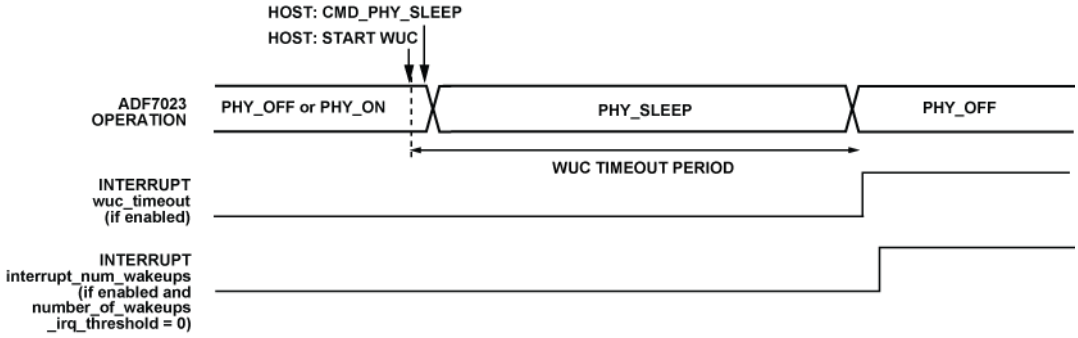


Figure 46. Low Power Mode Timing when just using the WUC

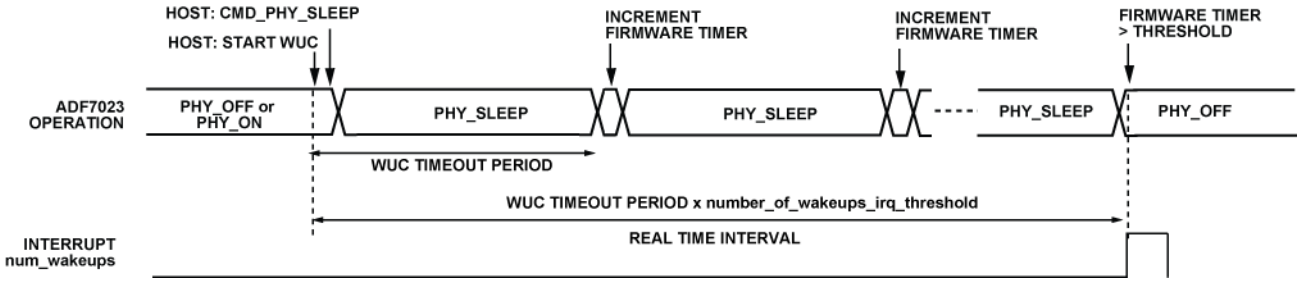


Figure 47. Low Power Mode Timing when using the WUC and the firmware timer

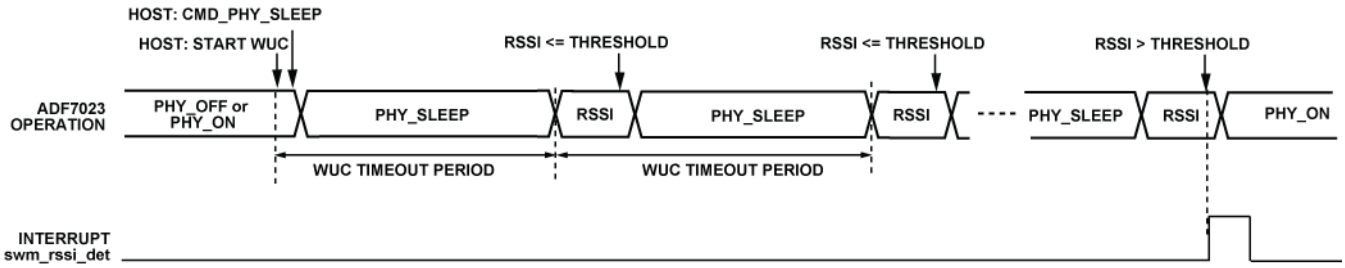


Figure 48. Low Power Mode Timing when using the WUC, the firmware timer and SWM with carrier sense only

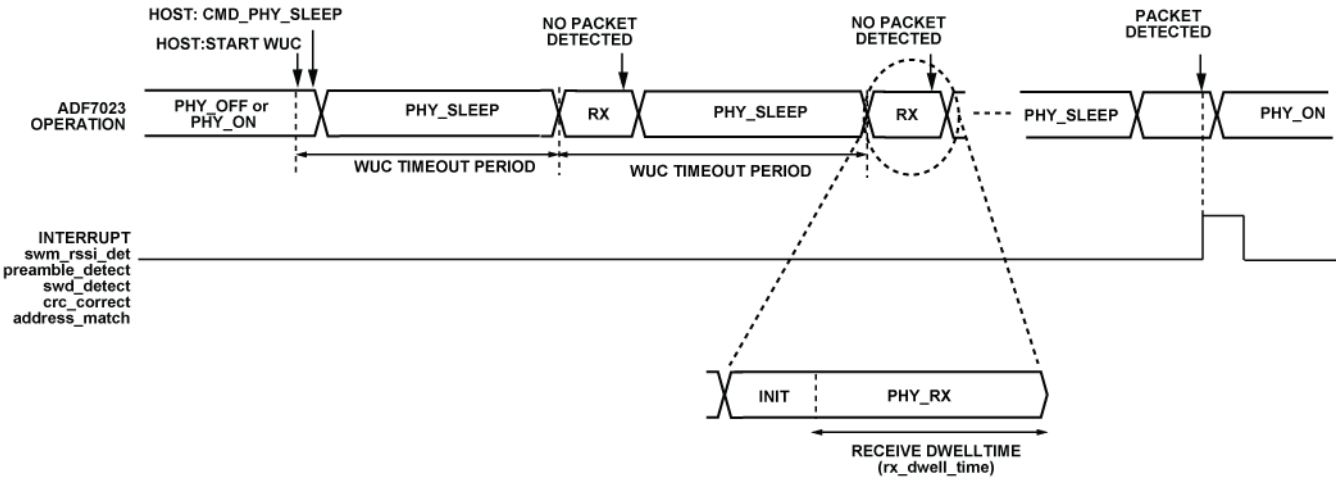


Figure 49. Low Power Mode Timing when using the WUC, the firmware timer and SWM

WUC SETUP

Circuit Description

The ADF7023 features a low power wake-up controller comprising of a 16-bit wake-up timer with a 3-bit programmable pre-scaler as illustrated in Figure 50. The pre-scaler clock source can be configured to use either the 32.768kHz internal RC oscillator (RCOSC) or the 32.768kHz external oscillator (XOSC). This combination of programmable pre-scaler and 16-bit down counter gives a total hardware timer range of 30.52us to 36.4 hours.

Configuration and Operation

The hardware WUC is configured via the following registers:

- wuc_config_high (location 0x30C)
- wuc _config_low (location 0x30D)
- wuc _value_high (location 0x30E)
- wuc _value_low (location 0x30F)

The relevant fields of each register are detailed in Table 26. All four of these registers are write only.

The WUC should be configured as follows:

1) Clear all interrupts
2) Set required interrupts
3) Write to wuc_config_high and wuc_config_low. Ensure that wuc_arm =1. Ensure wuc_config_low_bbram_en =1 (retain BBRAM during PHY_SLEEP). It is necessary to write to both registers together in the following order: wuc_config_high directly followed by writing to wuc_config_low.
4) Write to wuc_value_high and wuc_value_low. This sets the wuc_value[15:0] and thus the WUC timeout period. The timer will begin counting from the configured value once these registers has been written to. It is necessary to write to both registers together in the following order: wuc_value_high directly followed by writing to wuc_value_low.

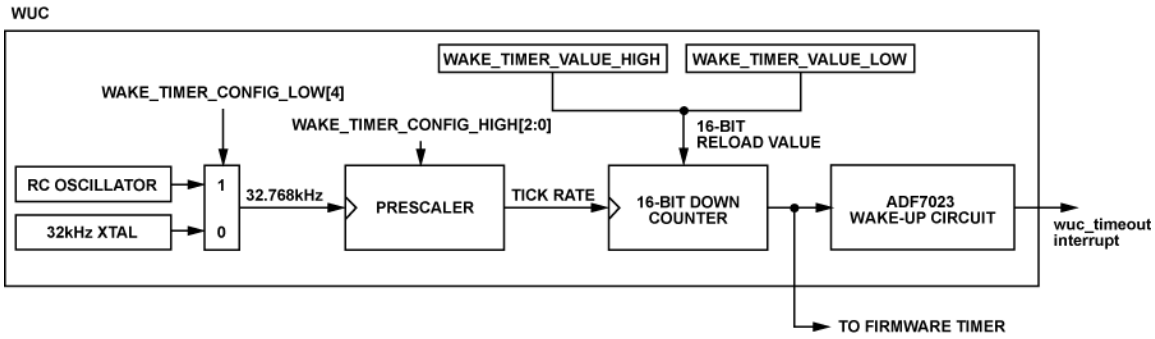


Figure 50. Hardware Wake Up Controller (WUC)

Table 26. WUC register settings

WUC Setting	Name	Description
wuc_value_high [7:0]	wuc_value [15:8]	WUC timer value. $\text{WUC interval (s)} = \frac{2^{(\text{wuc\_prescaler}+1)}}{32768}$
wuc_value_low [7:0]	wuc_value [7:0]	WUC timer value
wuc_config_high [7:3]	reserved	Set to 0
wuc_config_high [2:0]	wuc _prescaler	wuc_prescaler / 32.768kHz Divider / Tick Period: 000 / 1 / 30.52us; 001 / 4 / 122.1us; 010 / 8 / 244.1us; 011 / 16 / 488.3us; 100 / 128 / 3.91ms; 101 / 1034 / 31.25ms; 110 / 8192 / 250ms; 111 / 65536 / 2000ms
wuc_config_low[7]	reserved	Set to 0
wuc_config_low [6]	wuc _rcosc_en	1: enable; 0: disable RCOSC32K
wuc_config_low [5]	wuc _xosc32k_en	1: enable; 0: disable XOSC32K
wuc_config_low [4]	wuc _clksel	1: RC 32.768 kHz oscillator; 0: external crystal oscillator
wuc_config_low [3]	wuc _bbram_en	1: enable; 0: disable power to BBRAM during PHY_SLEEP

wuc_config_low [2:1]	reserved	Set to 0
wuc_config_low [0]	wuc_arm	1: enable; 0: disable wake-up on WUC timeout event

FIRMWARE TIMER SETUP

The ADF7023 will wake up from PHY_SLEEP at the rate set by the hardware WUC. A firmware timer, implemented by the on-chip processor, can be used to count the number of hardware wakeups. This firmware timer is used in smart wake mode to determine the number of hardware wakeups. The firmware timer can be used to generate an interrupt to the host microprocesor after a set number of ADF7023 wake ups. Thus, the ADF7023 can be used to handle the wake up timing of the host microprocessor, reducing overall system power consumption.

To set up the firmware timer, the host microprocessor must set the number_of_wakeups_irq_threshold[15:0] (location 0x104 and 0x105) to the desired value. This 16-bit value represents the number of times the device will wake up before it interrupts the host microprocessor. At each wake up, the ADF7023 will increment the number_of_wakeups[15:0]. If this value exceeds the value set by number_of_wakeups_irq_threshold[15:0]then the number_of_wakeups[15:0] value will be cleared to zero. At this time, if the interrupt_num_wakeups bit in interrupt_mask_1 (location 0x101) is set, then the device will assert the IRQ_GP3 pin and enter the state PHY_OFF.

DOWNLOADABLE FIRMWARE MODULES

The program RAM memory of the ADF7023 can be used to store firmware modules for the communications processor that provide extra functionality not already included in the ROM memory. The binary code for these firmware modules and detail on their functionality are available from ADI. Refer to the Program RAM Write section for details on how to download these software modules to program RAM. Three modules are briefly described here, namely, image rejection calibration, AES encryption and decryption and Reed-Solomon error correction.

MODULE: IMAGE REJECTION CALIBRATION

The calibration system initially disables the ADF7023 receiver, and an internal RF source is applied to the RF input at the image frequency. The algorithm then maximizes the receiver image rejection performance by iteratively minimizing the quadrature gain and phase errors in the polyphase filter.

The calibration algorithm takes its initial estimates for quadrature phase correction (location118) and quadrature gain correction (location 0x119) from BBRAM. After calibration, new optimum values of phase and gain are loaded back into these locations. These calibration values are maintained in BBRAM during sleep mode and are automatically reapplied from a wake-up event, which keeps the number of calibrations required to a minimum.

Depending on the initial values of quadrature gain and phase correction, the calibration algorithm can take approximately 20 ms to find the optimum image rejection performance. However, the calibration time can be significantly less than this when the seed values used for gain and phase correction are close to optimum.

The image rejection performance is also dependent on temperature. To maintain optimum image rejection performance, a calibration should be activated whenever a temperature change of more than 10°C occurs. The ADF7023 on-chip temperature sensor can be used to determine when the temperature exceeds this limit.

MODULE: REED SOLOMON CODING

This coding module uses systematic Reed-Solomon block coding to detect and correct errors in the received packet. A transmit message of k bytes in length, is appended with an error check code (ECC) of length n-k bytes to give a total message length of n bytes, as shown in Figure 51.

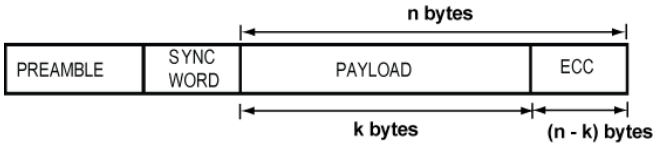


Figure 51. Packet structure with appended Reed-Solomon error check code (ECC)

The receiver decodes the ECC to detect and correct up to t byte errors in the received message where t = (n-k)/2. The downloadable firmware module supports a t value of between 1 and 5, allowing detection and correction of up to 5 byte errors with an ECC length of 10 bytes. The Reed-Solomon coding exhibits good burst error correction capability as it acts on byte symbols rather than on single bits. The total number of consecutive bit errors that can be corrected is = (t-1)×8+1. Therefore, with a 10 byte ECC (i.e. t=5), up to 33 consecutive bit errors can be corrected.

The firmware module utilizes on-chip hardware to accelerate the Reed Solomon encoding and decoding process.

MODULE: AES ENCRYPTION AND DECRYPTION

The downloadable AES firmware module supports 128 bit block encryption and decryption with key sizes of 128, 192 and 256 bits. Two modes are supported: ECB mode and CBC mode 1. ECB mode simply encrypts/decrypts on a 128 bit block by block with a single secret key as illustrated in Figure 52. CBC mode 1 encrypts after first adding (modulo 2) a 128 bit user supplied initialization vector. The resulting ciphertext is then used as the initialization vector for the next block and so forth as illustrated in Figure 53. Decryption provides the inverse functionality. The firmware module utilizes on-chip hardware to accelerate the encryption and decryption process.

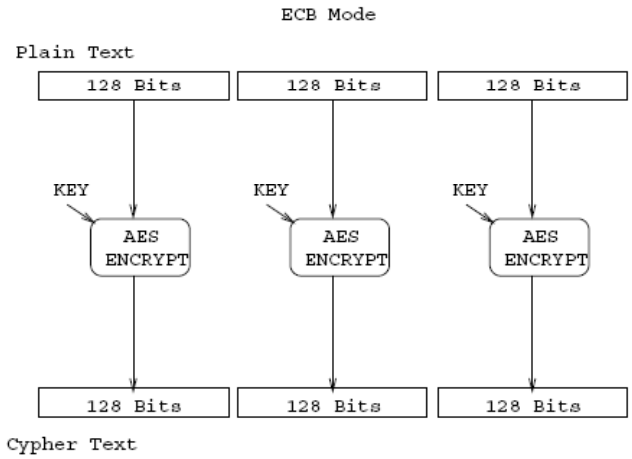


Figure 52 ECB Mode.

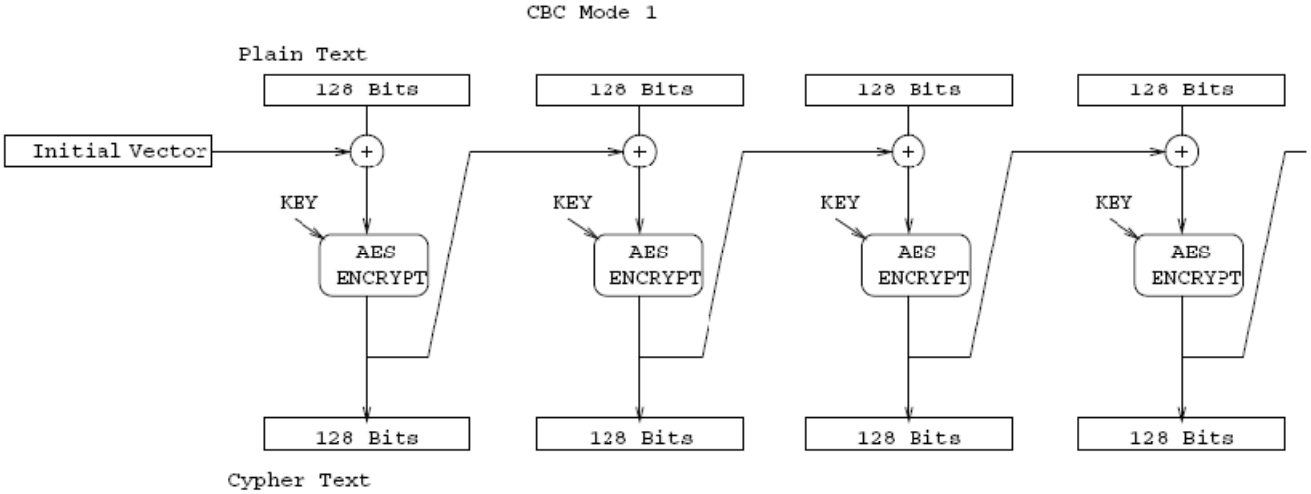


Figure 53. CBC1 Mode

RADIO BLOCKS

FREQUENCY SYNTHESIZER

A fully integrated RF frequency synthesizer is used to generate both the transmit signal and the receive local oscillator (LO) signal. The architecture of the frequency synthesizer is shown in Figure 54.

The receiver uses the synthesizer circuit to generate the LO for the receive down conversion to the intermediate frequency (IF) of 200 kHz or 300kHz. The transmitter uses a high resolution 100 Hz Σ-Δ modulator to generate the required frequency deviations at the RF when data is transmitted. The transmitted bit stream can be filtered using a Gaussian filter, which is enabled via the radio_cfg_9 register (location 0x115). The Gaussian filter uses a BT of 0.5.

The VCO and the PLL loop-filter of the ADF7023 are fully integrated. To reduce the effect of pulling of the VCO by the power-up of the PA and to minimize spurious emissions, the VCO operates at twice or four times the RF frequency. The VCO signal is then divided by 2 or 4, giving the required frequency for the transmitter and the required LO frequency for the receiver.

A fully automatic, high speed, frequency and amplitude VCO self-calibration scheme is employed to ensure that temperature, supply voltage, and process variations do not affect the VCO performance. The calibration is automatically performed upon issuing of the CMD_PHY_RX or CMD_PHY_TX command. The calibration is performed in 142 µs. If required, the calibration_status register (location 0x339) can be polled to indicate the completion of the VCO self-calibration. Once the VCO is calibrated, the frequency synthesizer can settle to within ±5 ppm of the target frequency in 56 µs in receive.

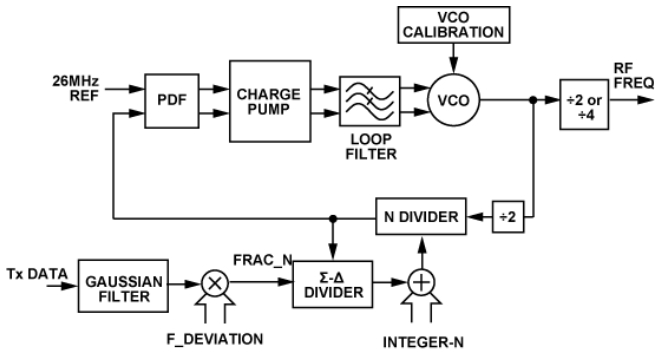


Figure 54. RF frequency synthesizer architecture

Synthesizer Bandwidth

The synthesizer loop filter, which is fully integrated on chip, has a programmable bandwidth. The communications processor automatically sets the bandwidth of the synthesizer when the device enters PHY_TX or PHY_RX. On entering PHY_TX the communications processor chooses the bandwidth based on the programmed modulation scheme (FSK/GFSK or OOK) and the data rate. This ensures optimum modulation quality for each data rate. On entering PHY_RX the communications processor sets a narrow bandwidth to ensure best receiver rejection. In all there are eight bandwidth configurations. Each synthesizer bandwidth setting is described in Table 27.

Table 27. Automatic synthesizer bandwidth selections

Description	Data rate (kbps)	Closed loop synthesizer bandwidth (kHz)
RX FSK/GFSK	All	92
TX FSK/GFSK	1 – 49.6	130
TX FSK/GFSK	49.7 – 99.2	174
TX FSK/GFSK	99.3 – 129.6	174
TX FSK/GFSK	129.7 – 179.2	226
TX FSK/GFSK	179.3 - 240	305
TX FSK/GFSK	240.1 - 300	382
TX OOK	All	185

Synthesizer Settling

After the VCO calibration, there a delay is required for synthesizer settling. This delay is fixed at 56us by default and ensures that the synthesizer has fully settled when using any of the default synthesizer bandwidths. However in some cases it may be necessary to use a custom sythsezier settling delay. To use a custom delay set the bit custom_trx_synth_lock_time_en = 1 (mode_control, location 0x11A). The synthesizer settling delays for the PHY_RX and PHY_TX state transitions can be set independently in rx_synth_lock_time (location 0x13E) and tx_synth_lock_time (location 0x13F). The settling time can be set in the range 2us to 512us in steps of 2us. The recommended settling times are detailed in Table 28.

Table 28. Recommended synthesizer settling

Description	Data rate (kbps)	Recommended Synthesizer settling (us)
RX FSK/GFSK	All	56 (default)
TX FSK/GFSK	1 – 49.6	TBD
TX FSK/GFSK	49.7 – 99.2	TBD
TX FSK/GFSK	99.3 – 129.6	TBD
TX FSK/GFSK	129.7 – 179.2	TBD
TX FSK/GFSK	179.3 - 240	TBD
TX FSK/GFSK	240.1 - 300	TBD
TX OOK	All	TBD

Bypassing VCO Calibration

It is possible to bypass the VCO calibration for ultra fast frequency hopping in transmit or receive. The calibration data for each RF channel should be stored in the host microprocessor memory. The calibration data comprises of two values: the VCO band select value and the VCO amplitude level.

Read and Store Calibration Data

- Go to PHY_TX or PHY_RX without bypassing the VCO calibration.

- Read the following MCR registers and store the calibrated data in memory on the host microprocessor:
  vco_band_readback (location 0x3DA)
  vco_ampl_readback (location 0x3DB)

Bypassing VCO Calibration on CMD_PHY_TX or CMD_PHY_RX

- Ensure the BBRAM is configured
- Set vco_ovrw_en = 0x3 (location 0x3CD)
- Set vco_cal_cfg = 0x0F (location 0x3D0)
- Set vco_band_ovrw_val = stored vco_band_readback for that channel
- Set vco_ampl_ovrw_val = stored vco_ampl_readback for that channel
- Set synth_cal_en = 0 (in register calibration_control, location 0x338)
- Set synth_cal_en = 1 (in register calibration_control, location 0x338)
- Issue CMD_PHY_TX or CMD_PHY_RX to go to PHY_TX or PHY_RX without the VCO calibration

MODULATION

The ADF7023 supports binary frequency shift keying (FSK), minimum shift keying (MSK), binary level Gaussian filtered FSK (GFSK), Gaussian filtered MSK (GMSK) and On-Off Keying (OOK). The desired transmit and receive modulation formats are set in register radio_cfg_9 (location 0x115). The Gaussian filter uses a fixed Bandwidth-Time (BT) product of 0.5. The frequency deviation can be set using the freq_deviation[11:0] parameter in registers radio_cfg_1 (location 0x10D) and radio_cfg_1 (location 0x10E). The data rate can be set in the range 0.1kbps to 300kbps using the data_rate[11:0] parameter in registers radio_cfg_0 (location 0x10C) and radio_cfg_1 (location 0x10D). It is necessary to use Manchester encoding with OOK modulation.

RF OUTPUT STAGE

Power Amplifier (PA)

The PA of the ADF7023 can be used either in a single-ended configuration or with a differential output configuration. The choice of PA is set by the bit pa_single_diff_sel (radio_cfg_8, location 0x114). The PA level is set by pa_power (radio_cfg_8, location 0x114) and has a range from 0 to 15. However the register pa_level_mcr (location 0x307) can also be used to set the PA level but with more resolution as it has a range of 0 to 63. Both settings are related by pa_level_mcr = 4×pa_level + 3.

The single-ended configuration can deliver 13.5 dBm output power. The differential PA can deliver 10 dBm output power. and allows straightforward interfacing to dipole antennas. The two PA configurations offer a Tx antenna diversity capability. The two PAs cannot be on at the same time.

Automatic PA Ramp

The ADF7023 has built-in up and down PA ramping for both single-ended and differential PAs. There are eight ramp rate settings, defined as a certain number of PA power level settings for each data bit period. The PA steps through each PA code setting, at a rate defined by the pa_ramp variable (radio_cfg_8, location 0x114), as illustrated in Figure 55.

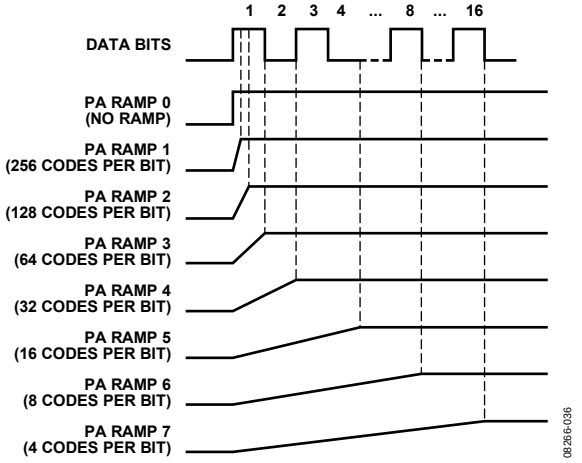


Figure 55. PA ramp for different pa_ramp settings

The PA ramps to the level set by the pa_level or pa_level_mcr settings. Enabling the PA ramp reduces spectral splatter and helps in meeting radio regulations (for example, the ETSI EN 300 220 standard), which limit PA transient spurs. The PA ramps down at the same rate. To ensure optimum performance an adequately long PA ramp rate is required based on the data rate and the PA output power setting. The pa_ramp setting should therefore be set such that:

$$pa\_ramp[2:0] > 11 - \log_2\left[\frac{10000 \times pa\_mcr\_level[7:0]}{data\_rate[11:0]}\right]$$

Where pa_mcr_level is related to the pa_level setting by pa_level_mcr = 4×pa_level + 3.

PA/LNA INTERFACE

The LNA of the ADF7023 has a differential input while there is the option of a single-ended output PA or a differential output PA. The differential PA and LNA use the same pins, RFIO_1P and RFIO_1N, which facilities a simpler antenna interface. The single-ended PA output is on pin RF02, while the bias for the PA is provided from pin CREGRF2. Various PA and LNA matching options are possible and are described in the PA/LNA section.

RECEIVE CHANNEL FILTER

The receiver IF filter is a fourth-order, active Butterworth, polyphase filter centered at the IF frequency of 200 kHz or 300kHz (depending on the bandwidth setting). The receiver image frequency, which is 400 kHz (IF bandwidth = 100kHz to 200kHz) or 600kHz (IF bandwidth = 300kHz) below the desired signal, is rejected by the polyphase filter. The IF filter bandwidth and center frequency are calibrated automatically

after entering the PHY_ON state if the bb_cal bit is set (mode_control, location 0x11A). The calibration is required and takes 100 µs.

The receiver IF filter bandwidth has programmable settings of 100, 150, 200 and 300 kHz and is set by the ifbw setting (radio_cfg_9, location 0x115). The IF filter is centered at 200kHz when a bandwidth of 100, 150 or 200kHz is used and is centered at 300kHz when a bandwidth of 300kHz is used.

IMAGE CHANNEL REJECTION

The ADF7023 is capable of providing improved image rejection performance by the use of a fully integrated image rejection calibration system, combined with a firmware download that is written to the in the on-chip program RAM and is run by the communications processor. The firmware download is supplied by Analog Devices, Inc and described in the Downloadable Firmware Modules section.

AUTOMATIC GAIN CONTROL (AGC)

AGC is enabled by default, and keeps the receiver gain at the correct level by selecting the LNA, mixer and filter gain settings based on the measured RSSI level. The LNA has three gain levels, the mixer two levels, and the filter 3 gain levels. In all there are six AGC stages which are defined in Table 29.

Table 29. AGC Gain Modes

Gain Mode	LNA gain	Mixer Gain	Filter Gain
1	High	High	High
2	High	Low	High
3	Medium	Low	High
4	Low	Low	High
5	Low	Low	Medium
6	Low	Low	Low

The AGC remains at each gain stage for a time of 25us before deciding on whether to change the gain based on the measured RSSI. The 25us allows for settling of the RSSI signal after a gain change. The time is set to 25us by default but can be changed in the agc_clk_divide register (location 0x32F).

The AGC can be configured to remain active while in PHY_RX or it can be locked on preamble detection. The AGC can also be set to manual mode in which case the host microprocessor must set the LNA, filter and mixer gains by writing to register agc_mode (location 0x35D). The AGC operation is set by the agc_operation setting (radio_cfg_7, location 0x113) and is described in Table 30.

The LNA, filter and mixer gains can be readback through the agc_gain_status register (location0x360).

Table 30. AGC Operation

agc_operation (0x113)	Description
0	AGC is free running
1	AGC is disabled. Gains must be set manually
2	AGC is held at current gain level
3	AGC is locked on preamble detection

RSSI

The RSSI is implemented as a successive compression log amp following the IF channel filtering. The RSSI level is converted for user readback and for the digitally controlled AGC by an 8-bit SAR ADC. The three methods to read the RSSI level are detailed here.

RSSI on packet in FSK/GFSK

When a valid packet is received (in packet mode) the RSSI level is automatically loaded to the rssi_readback register (location 0x312) by the communications processor. The rssi_readback is a 2s complement binary value and can be converted to input power in dBm using the formula:

Input Power (dBm) = rssi_readback- 107

CMD_GET_RSSI

The CMD_GET_RSSI can be used from PHY_ON to read the RSSI. This RSSI measuremrnt method uses eadditional low pass filtering of the RSSI and thus can give a more accurate RSSI reading. The RSSI result is loaded to the rssi_readback register.

RSSI in SPORT mode

Another method to read the RSSI, while in PHY_RX and using FSK/GFSK modulation, is to readback the AGC gain and the ADC level. This is the recommended RSSI readback method when operating in SPORT mode. The receiver input power can be calculated using the following procedure:

- Set AGC to freeze by setting register 0x35D = 0x40 (only necessary if AGC has not been locked on preamble)
- Readback RF front end gain settings:
  Read agc_gain_status (location 0x360)
- Do a random access read of the ADC readback registers in the following sequence
  1. Read adc_readback_high (location 0x327). This initializes an ADC readback.
  2. Read adc_readback_low. This returns the least significant bits of the ADC sample. i.e. adc_code[2:0]
  3. Read adc_readback_high. This returns the most significant bits of the ADC sample. adc_code[8:3]
- Re-enable the AGC:
  Set register 0x35D = 0x00 (Only necessary if AGC has not been locked on preamble)
- $Rx\ input\ power\ (dBm) =$

$$\frac{adc\_readback[7:0]}{6.765} - 109.21 + 9.25 \times (gain\_mode - 1)$$

where the adc_readback value is read from registers 0x327 and 0x328 and the AGC gain_mode is determined using the value in agc_gain_status (location 0x360) and Table 29.

FSK/GFSK/MSK/GMSK DEMODULATION

A correlator demodulator is used for FSK, MSK, GFSK and GMSK demodulation. The quadrature outputs of the IF filter are first limited and then fed to a digital frequency correlator that performs filtering and frequency discrimination of the 2FSK or GFSK spectrum. For 2FSK/GFSK modulation, data is recovered by comparing the output levels from two correlators. The performance of this frequency discriminator approximates that of a matched filter detector, which is known to provide optimum detection in the presence of additive white Gaussian noise (AWGN). This method of FSK/GFSK demodulation provides approximately 3 dB to 4 dB better sensitivity than a linear frequency discriminator. The FSK/GSK demodulator architecture is shown in Figure 56. The ADF7023 is set for FSK/GFSK demodulation by setting demod_scheme = 0 (radio_cfg_9, location 0x115).

To optimize receiver sensitivity, the correlator bandwidth and phase must be optimized for the specific deviation frequency, data rate and maximum expected frequency error between the transmitter and receiver. The bandwidth and phase of the discriminator must be set using the discrim_bw (radio_cfg_3, location 0x10F) and discrim_phase[9:0] (radio_cfg_5 and radio_cfg_6, location 0x111 and 0x112). The discriminator setup is performed in 3 steps:

Step 1: Calculate the discriminator bandwidth coefficient K

The discriminator bandwidth coefficient K depends on the modulation index (MI) which is determined by:

$$MI = \frac{2 \times FSK\_dev}{datarate}$$

Where FSK_dev is the FSK/GFSK frequency deviation in Hz, measured from the carrier to the one (+ deviation) or zero (- deviation) frequency, and datarate is the data rate in bps. The value of K is then determined by:

$$MI \geq 1, \qquad K = Floor\left[\frac{IF\_freq}{FSK\_dev + Freq\_error\_max}\right]$$

$$MI < 1, \qquad K = Floor\left[\frac{IF\_freq}{\frac{datarate}{2} + Freq\_error\_max}\right]$$

Where MI is the modulation index, K is the discriminator coefficient, Floor[] is a function to round down to the nearest integer, IF_freq is the IF frequency in Hz (200kHz or 300kHz), FSK_dev is the FSK/GFSK frequency deviation in Hz and Freq_error_max is the maximum expected frequency error, in Hz, between Tx and Rx.

Step 2: Calculate the discrim_bw setting

The bandwidth setting of the discriminator is calculated based on the discriminator coefficient K and the IF frequency. The bandwidth is set using discrim_bw setting (location 0x10F) which is calculated according to:

$$discrim\_bw[7:0] = Round\left[\frac{K \times 3.25MHz}{IF\_freq}\right]$$

Step 3: Calculate the discrim_phase setting

The phase setting of the discriminator is calculated based on the discriminator coefficient K as described in Table 31. The phase is set using the discrim_phase[1:0] value (radio_cfg_6, location 0x112).

Table 31. Setting the discrim_phase[1:0] value based on K

K	K/2	(K+1)/2	discrim_phase [1:0]
even	odd	-	0
even	even	-	1
odd	-	even	2
odd	-	odd	3

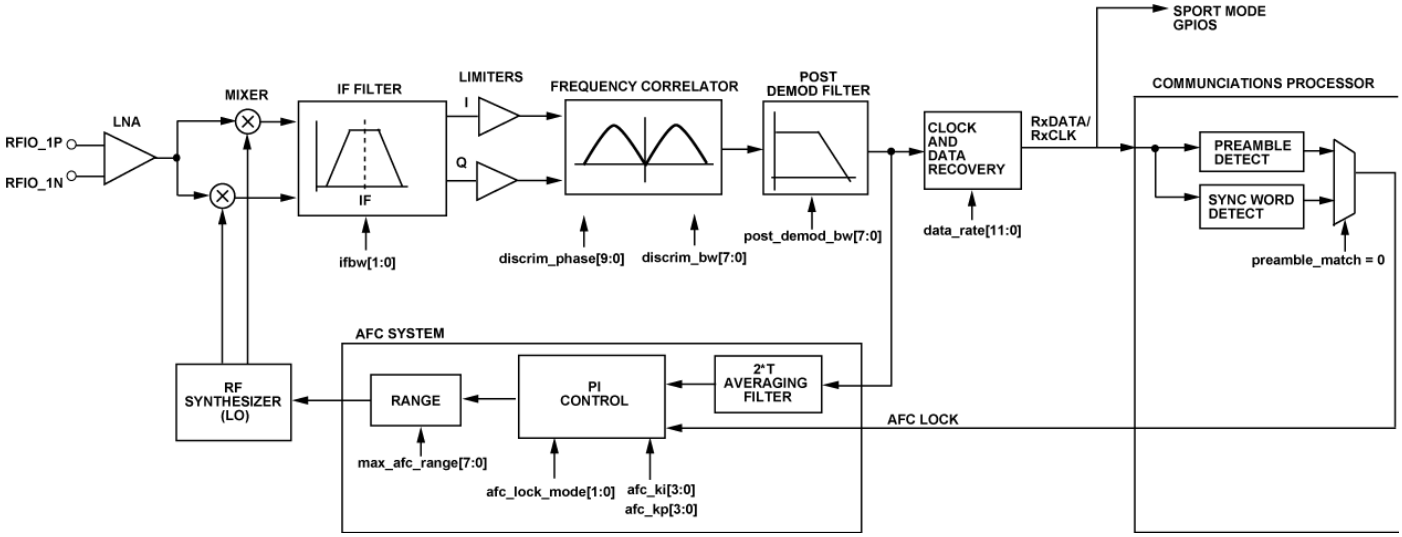


Figure 56. FSK/GFSK Demodulation and AFC Architecture

AFC

The ADF7023 supports a real-time, internal, automatic frequency control loop. In receive, an internal control loop automatically monitors the frequency error during the packet preamble sequence and adjusts the receiver synthesizer LO using an internal proportional integral (PI) control loop. The AFC frequency error measurement bandwidth is targeted specifically at the packet preamble sequence (DC Free). Once preamble is detected, the AFC is locked by the communications processor. AFC lock is released if sync word is not detected immediately after the end of preamble. If the qualified preamble is followed by a qualified sync word, the AFC lock is maintained for the duration of the packet.

AFC can also be configured to lock on sync word detection (set preamble_match = 0, location 0x11B). If this mode is selected then consideration must be given to the selection of sync word. The sync word should be DC-free, have short run lengths yet have low correlation with the preamble sequence.

AFC is enabled by setting afc_lock_mode (radio_cfg_10, location: 0x116) as described in Table 34

Table 32. AFC mode

afc_lock_mode[1:0]	Mode
0	Free Running: AFC is free running
1	Disabled: AFC is disabled
2	Hold: AFC is paused
3	Lock: AFC locks after preamble or SWD

The bandwidth of the AFC loop can be controlled by the afc_ki and afc_kp parameters (radio_cfg_11, 0x117).
The maximum AFC pull in range is automatically set based on the programmed IF filter bandwidth (ifbw in register radio_cfg_9, location 0x115).

Table 33. Maximum AFC pull in range

IF Bandwidth	Max AFC pull in range
100kHz	±50kHz
150kHz	±75kHz
200kHz	±100kHz
300kHz	±150kHz

AFC and Preamble Length

The AFC will require a certain number of the received preamble bits to correct the frequency error between the transmitter and the receiver. The number of preamble bits required depends on whether the AFC is locked on detection of preamble or locked on detection of sync word. When AFC is locked on preamble detection the preamble will typically need to be 40 to 60 bits in length, depending on the data rate. When AFC is set to lock on sync word detection, the typical preamble length needs to be 20 to 40 bits, depending on the data rate. When AFC is disabled the typical preamble length is dependant on the AGC settling and the clock and data recovery. With AFC disabled and preamble detection disabled the typical required preamble length is 12 – 30 bits.

AFC Readback

The frequency error between the received signal frequency and the Rx LO can be measured when AFC is enabled. The error value can be read from the frequency_error_readback register (location 0x372), where each LSB equates to 1kHz. The value is a 2s complement number. The frequency_error_readback value is valid in PHY_RX once preamble has been detected. The value is retained in the frequency_error_readback register after recovering a packet and transitioning back to PHY_ON.

Post-demodulator Filter

A second-order, digital low-pass filter removes excess noise from the demodulated bit stream at the output of the discriminator. The bandwidth of this post-demodulator filter is programmable and must be optimized for the user's data rate and received modulation type. If the bandwidth is set too narrow, performance degrades due to intersymbol interference (ISI). If the bandwidth is set too wide, excess noise degrades the performance of the receiver. For optimum performance, the post-demodulator filter bandwidth should be set to 0.75 times the data rate:

$$post\_demod\_bw = Round[(7.5 \times 10^{-4} \times datarate \times 0.73) - 5]$$

Where datarate is the data rate in bps.

Clock Recovery

An oversampled digital Clock and Data Recovery (CDR) PLL is used to resynchronize the received bit stream to a local clock in all modulation modes. The maximum symbol rate tolerance of the CDR PLL is determined by the number of bit transitions in the transmitted bit stream. For example, during reception of a 010101 preamble, the CDR achieves a maximum data rate tolerance of ±3.0%. However, this tolerance is reduced during recovery of the remainder of the packet where symbol transitions may not be guaranteed to occur at regular intervals during the payload data. To maximize data rate tolerance of the receiver's CDR, 8b10b encoding or Manchester encoding should be enabled which guarantee a maximum number of contiguous bits in the transmitted bit stream. Data whitening can also be enabled on the ADF7023 to break up long sequence of contiguous data bit patterns.

Using FSK/GFSK modulation, it is also possible to tolerate uncoded payload data fields and payload data fields with long run length coding constraints if the data rate tolerance and packet length are both constrained. More details of CDR operation using uncoded packet formats are discussed in application note AN-915.

The ADF7023's CDR PLL has been optimized for fast acquisition of the recovered symbols during preamble and typically achieves bit synchronization within 5-symbol transitions of preamble.

OOK DEMODULATION

The ADF7023 is set for OOK demodulation by setting demod_scheme = 2 (radio_cfg_9, location 0x115). Manchester encoding must be used with OOK modulation to ensure correct data demodulation. The AGC and AFC should be set to lock after preamble detection by setting the agc_lock_mode = 3 (radio_cfg_7, location 0x113) and afc_lock_mode = 3 (radio_cfg_10, location 0x116).

CRYSTAL OSCILLATOR

A 26 MHz crystal oscillator operating in parallel mode must be connected between the XOSC26P and XOSC26N pins. Two parallel loading capacitors are required for oscillation at the correct frequency. Their values are dependent upon the crystal specification. They should be chosen to ensure that the shunt value of capacitance added to the PCB track capacitance and the input pin capacitance of the ADF7023 equals the specified load capacitance of the crystal, usually 10 pF to 20 pF. Track capacitance values vary from 2 pF to 5 pF, depending on board layout. The input pin capacitance of the ADf7023 is about 3pF on each pin. The total load capacitance is described by:

$$C_{LOAD} = \frac{1}{\frac{1}{C_1} + \frac{1}{C_2}} + C_{PIN} + C_{PCB}$$

Where C_{LOAD} is the total load capacitance, C_{PIN} is the ADF7023 input pin capacitance (=1.5pF typical) and C_{PCB} is the PCB track capacitance. When possible, choose capacitors that have a very low temperature coefficient to ensure stable frequency operation over all conditions.

The crystal frequency error can be corrected by means of an integrated digital tuning varactor. A tuning range of −15 ppm to +11.25 ppm is available via programming of a 3-bit DAC, according to Table 34. The 3-bit value should be written to xosc_cap_dac (osc_and_doubler_config, location 0x3D2).

Alternatively, any error in the RF frequency due to crystal error, can be adjusted for by offsetting the RF channel frequency using the BBRAM RF channel frequency settings.

Table 34. Crystal Frequency Pulling Programming

xosc_cap_dac	Pulling (ppm)
000	−15
001	−11.25
010	−7.5
011	−3.75
100	0
101	+3.75
110	+7.5
111	+11.25

PERIPHERAL FEATURES

ANALOG-TO-DIGITAL CONVERTER

The ADF7023 supports an integrated SAR ADC for digitization of analog signals that include the analog temperature sensor, the analog RSSI level, and an external analog input signal (Pin 30). The conversion time is typically 1 µs. The result of the conversion can be read from register adc_readback_high (location 0x327), and register adc_readback_low (location 0x328). The ADC readback is an 8-bit value.

The signal source for the ADC input is selected via the adc_config_low register (location 0x359). In PHY_RX the source is automatically set to the analog RSSI. To perform a readback, the following procedure should be followed:

- Read adc_readback_high.
  This initializes an ADC readback.
- Read adc_readback_low.
  This returns adc_readback[2:0] of the ADC sample.
- Read adc_readback_high.
  This returns adc_readback[7:3] of the ADC sample.

Temperature Sensor

The integrated temperature sensor has an operating range between −40°C and +85°C. The temperature sensor is enabled via the powerdown_aux register (location 0x325). The temperature is determined from the readback value using the following formula:

Temperature (°C) = (*adc_readback[7:0]*/35) − 118.43 + *Correction Value*

The correction value can be determined by performing a readback at a single known temperature. When this correction is applied, the temperature sensor is accurate to ±14°C over the full operating temperature range. Averaging a number of ADC readbacks can improve the accuracy of the temperature measurement. If an average of 10 readbacks is taken, the accuracy improves to ±4.4°C.

Test DAC

The test DAC allows the output of the post-demodulator filter to be viewed externally. It takes the 16-bit filter output and converts it to a high frequency, single-bit output using a second-order Σ-Δ converter. The output can be viewed on the GP0 pin. This signal, when filtered appropriately, can be used to

- Monitor the signal at the post-demodulator filter output.
- Measure the demodulator output SNR.
- Construct and eye diagram of the received bit stream to measure the received signal quality.
- Implement analog FM demodulation.

To enable the test DAC the gpio_configure setting (location 0x3FA) should be set to 0xC9. The test_dac_gain setting (location 0x3FD) should be set to 0x00. The test DAC signal at the GP0 pin can be filtered with a 3-stage low-pass RC filter to reconstruct the demodulated signal. For further information, refer to the application note AN-852.

TRANSMIT TEST MODES

There are two transmit test modes which are enabled by setting the var_tx_mode parameter (location 0x00D) as described in Table 35. The var_tx_mode setting should be set before entering PHY_TX.

Table 35. Transmit test modes

var_tx_mode	Mode
0	Default. No transmit test mode
1	reserved
2	Transmit preamble continuously
3	Transmit carrier continuously
4 to 255	reserved

APPLICATIONS INFORMATION

APPLICATIONS CIRCUIT

A typical application circuit for the ADF7023 is shown in Figure 57. All external components required for operation of the device, excluding supply decoupling capacitors are shown. This example circuit uses a combined single-ended PA and LNA match. Further details on matching topologies and different host microprocessor interfaces are given in the following sections.

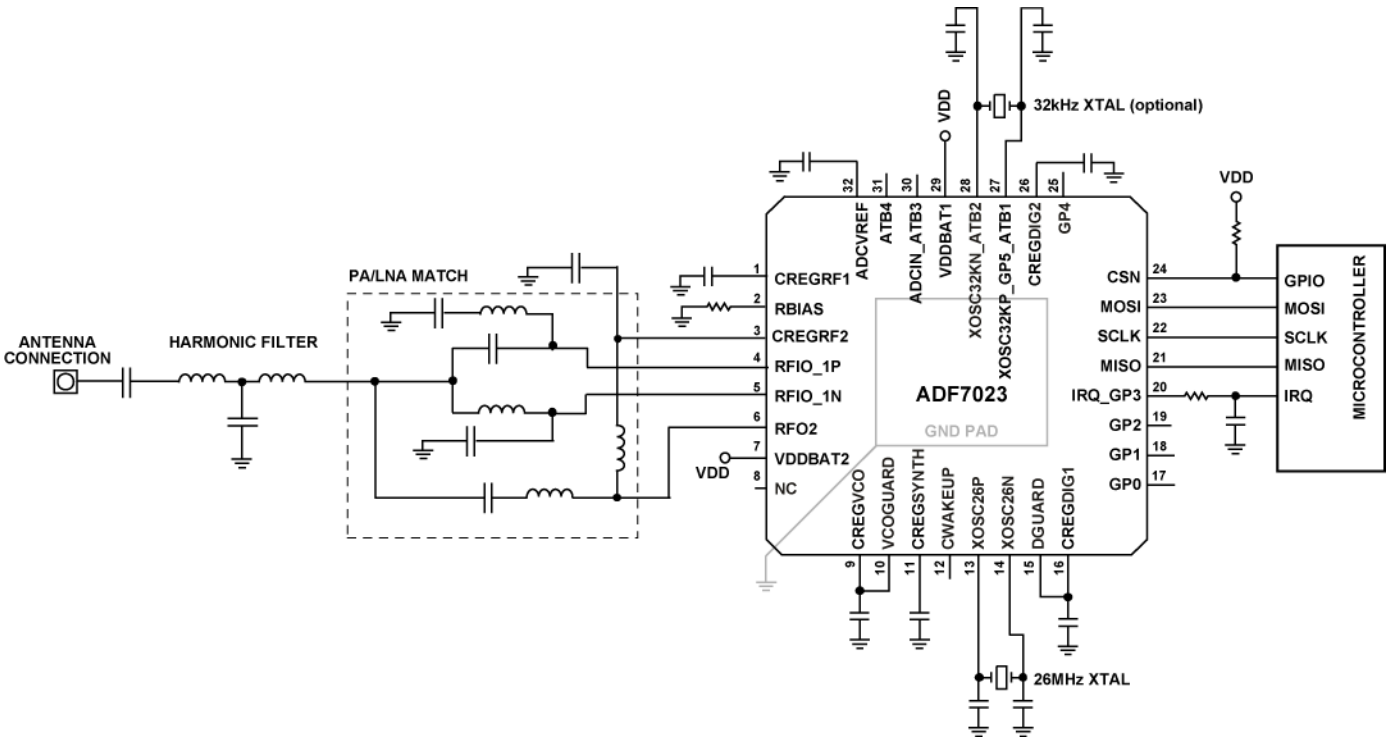


Figure 57. Typical ADF7023 Application Circuit Diagram

MICROPROCESSOR INTERFACE

The interface between the ADF7023 and the host microcontroller will depend on whether or not SPORT mode is being used. The standard interface is shown in Figure 58, where all communication is via the SPI interface. In SPORT mode, the transmit and receive data interface is the GP0, GP1 and GP2 pins while a separate interrupt for SPORT mode is available on GP4. The SPI interface is used as normal for memory access and issuing of commands in SPORT mode as shown in Figure 59.

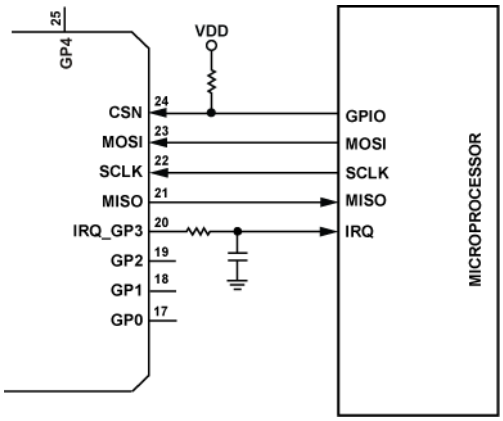


Figure 58. Microprocessor interface in packet mode

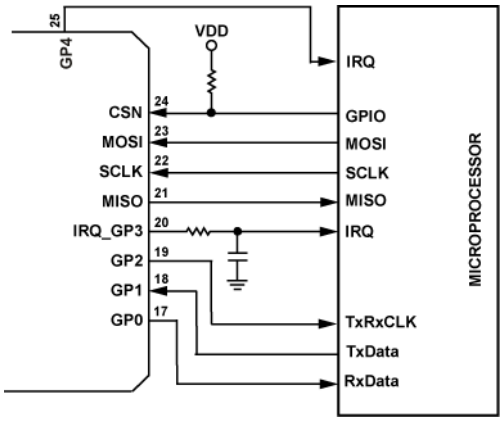


Figure 59. Microprocessor interface in SPORT mode

PA/LNA INTERFACE

The AD7023 has a differential LNA and both a single-ended PA and differential PA. This flexibility allows numerous possibilities in interfacing the ADF7023 to the antenna.

Combined Single-Ended PA and LNA Match

This combined single-ended PA and LNA match allows the transmit and receive paths to be combined without the use of an external transmit/receive switch. The matching network design is shown in Figure 60. The differential LNA match is a five element discrete balun giving a single-ended input. The single-ended PA output is a three element match consisting of the choke inductor to the CREGRF2 regulated supply and a series inductor and capacitor. The LNA and PA paths are combined and a T-stage harmonic filter provides attenuation of the transmit harmonics.

In a combined match the off impedances of the PA and LNA need to be considered. This can lead to a small loss in transmit power and degradation in receiver sensitivity in comparison with a separate single-ended PA and LNA match. However, with optimum matching, the typical loss in transmit power is <1dB and the degradation in sensitivity is < 1dB when compared with a separate PA and LNA matching topology.

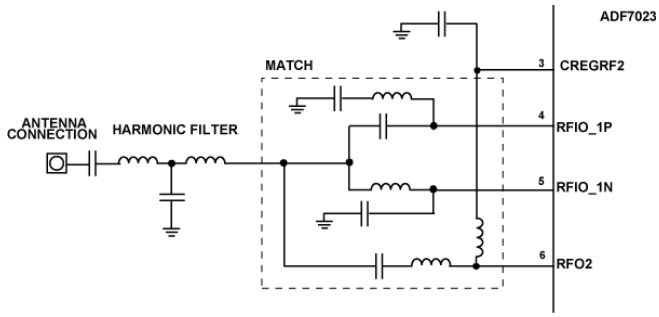


Figure 60. Combined single-ended PA and LNA match

Separate Single-ended PA/LNA Match

The separate single-ended PA and LNA matching configuration is illustrated in Figure 61. The network is the same as the combined matching network shown in Figure 60 except the transmit and receive paths are separate. An external transmit/receive antenna switch can be used to combine the transmit and receive paths to allow connection to an antenna. In designing this matching network it is not necessary to consider the off impedances of the PA and LNA and thus achieving an optimum match is less complex than the combined single-ended PA and LNA match.

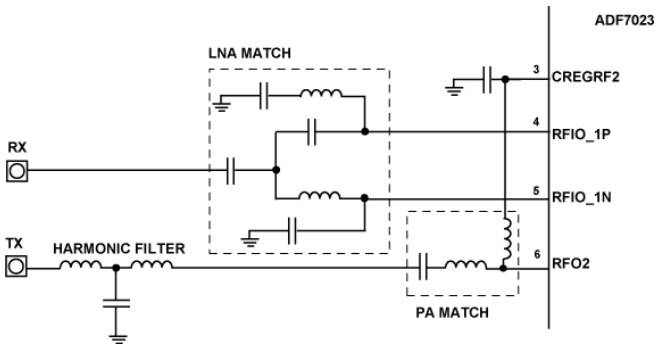


Figure 61. Separate single-ended PA and LNA match

Combined Differential PA/LNA Match

In this matching topology the single ended PA is not used. The differential PA and LNA match comprises of a five element discrete balun giving a single-ended input/output as illustrated in Figure 62. The harmonic filter is used to minimize the RF harmonics from the differential PA.

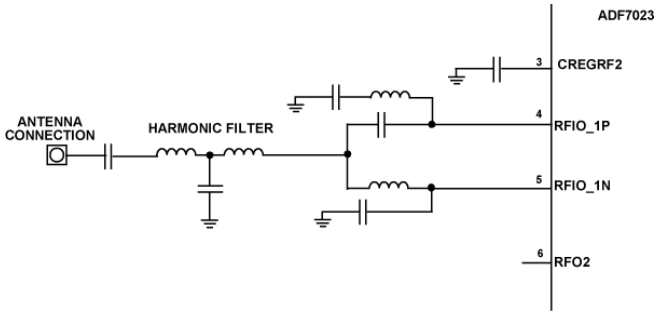


Figure 62. Combined differential PA and LNA match

Transmit Antenna Diversity

Transmit antenna diversity is possible using the differential PA and single ended PA. The required matching networks is shown in Figure 63.

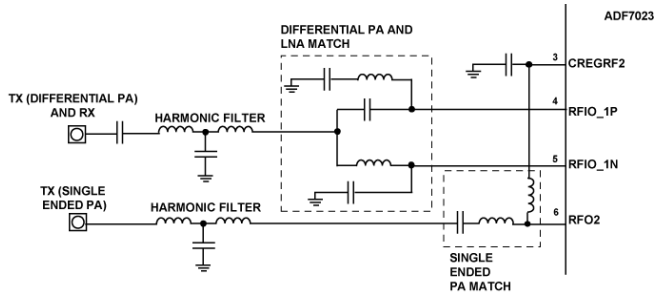


Figure 63. Matching topology for transmit antenna diversity

Support for External PA and LNA Control

The ADF7023 provides independent enable signals for an external PA or LNA. If the ext_pa_en bit is set to one (mode_control, location 0x11A), then the ADCIN_ATB3 pin will be logic high while the ADF7023 is in the PHY_TX state and will be logic low while in any other state. If the ext_lna_en bit is set to one (mode_control, location 0x11A), then the ATB4 pin will be logic high while the ADF7023 is in the PHY_RX state and will be logic low while in any other state.

COMMAND REFERENCE

Table 36. ADF7023 Radio Controller commands

Commands	Code	Description
CMD_SYNC	0xA2	Synchronizes the communication processor to the host microprocessor after rest
CMD_PHY_OFF	0xB0	Invoke transition of device into state PHY_OFF
CMD_PHY_ON	0xB1	Invoke transition of device into state PHY_ON
CMD_PHY_RX	0xB2	Invoke transition of device into state PHY_RX
CMD_PHY_TX	0xB5	Invoke transition of device into state PHY_TX
CMD_PHY_SLEEP	0xBA	Invoke transition of device into state PHY_SLEEP
CMD_CONFIG_DEV	0xBB	Configures the radio parameters based on the BBRAM values.
CMD_GET_RSSI	0xBC	Performs an RSSI measurement
CMD_BB_CAL	0xBE	Performs an calibration of the IF filter
CMD_HW_RESET	0xC8	Performs a full hardware reset. The device enters PHY_SLEEP
CMD_RAM_LOAD_INIT	0xBF	Prepares the program RAM for a download
CMD_RAM_LOAD_DONE	0xC7	Performs a reset of the communications processor after loading RAM
CMD_IR_CAL	0xBD	Initiates an image rejection calibration using the IR cal code stored on program RAM
CMD_AES_ENCRYPT	0xD0	Perform an AES encryption using the AES code stored on program RAM
CMD_AES_DECRYPT	0xD1	Perform an AES decryption using the AES code stored on program RAM
CMD_AES_DECRYPT_INIT	0xD2	Setup an AES decryption using the AES code stored on program RAM

Table 37. ADF7023 SPI commands

Commands	Code	Description
SPI_MEM_WR	00011xxxb = 0x18 (packet RAM) = 0x19 (BBRAM) = 0x1B (MCR) = 0x1A (program RAM)	Write data to BBRAM/MCR or Packet RAM sequentially. An 11 bit address is used to identify memory locations. The most significant 3 bits of the address are incorporated in to the command (xxxb). This command is followed by the remaining 8 bits of the address.
SPI_MEM_RD	00111xxxb = 0x38 (packet RAM) = 0x39 (BBRAM) = 0x3B (MCR)	Read data from BBRAM/MCR or Packet RAM sequentially. An 11 bit address is used to identify memory locations. The most significant 3 bits of the address are incorporated in to the command (xxxb). This command is followed by the remaining 8 bits of the address, which is subsequently followed by the appropriate number of SPI_NOP commands.
SPI_MEMR_WR	00001xxxb = 0x08 (packet RAM) = 0x09 (BBRAM) = 0x0B (MCR)	Write data to BBRAM/MCR or Packet RAM at random.
SPI_MEMR_RD	00101xxxb = 0x28 (packet RAM) = 0x29 (BBRAM) = 0x2B (MCR)	Read data from BBRAM/MCR or Packet RAM at random.
SPI_NOP	= 0xFF	No operation. Use for dummy writes when polling the status word. Used also as dummy data on the when performing a memory read.

REGISTER MAPS

Table 38. Battery Backup Memory (BBRAM)

Address (Hex)	Register	Retained in PHY_SLEEP	R/W	Group
0x100	interrupt_mask_0	Yes	R/W	MAC
0x101	interrupt_mask_1	Yes	R/W	MAC
0x102	number_of_wakeups_0	Yes	R/W	MAC
0x103	number_of_wakeups_1	Yes	R/W	MAC
0x104	number_of_wakeups_irq_threshold_0	Yes	R/W	MAC
0x105	number_of_wakeups_irq_threshold_1	Yes	R/W	MAC
0x106	max_wakeup_2_sync_time	Yes	R/W	MAC
0x107	parmtime_divider	Yes	R/W	MAC
0x108	swm_rssi_thresh	Yes	R/W	PHY
0x109	channel_freq_0	Yes	R/W	PHY
0x10A	channel_freq_1	Yes	R/W	PHY
0x10B	channel_freq_2	Yes	R/W	PHY
0x10C	radio_cfg_0	Yes	R/W	PHY
0x10D	radio_cfg_1	Yes	R/W	PHY
0x10E	radio_cfg_2	Yes	R/W	PHY
0x10F	radio_cfg_3	Yes	R/W	PHY
0x110	radio_cfg_4	Yes	R/W	PHY
0x111	radio_cfg_5	Yes	R/W	PHY
0x112	radio_cfg_6	Yes	R/W	PHY
0x113	radio_cfg_7	Yes	R/W	PHY
0x114	radio_cfg_8	Yes	R/W	PHY
0x115	radio_cfg_9	Yes	R/W	PHY
0x116	radio_cfg_10	Yes	R/W	PHY
0x117	radio_cfg_11	Yes	R/W	PHY
0x118	image_reject_cal_phase	Yes	R/W	PHY
0x119	image_reject_cal_amplitude	Yes	R/W	PHY
0x11A	mode_control	Yes	R/W	PHY
0x11B	preamble_match	Yes	R/W	Packet
0x11C	symbol_mode	Yes	R/W	Packet
0x11D	preamble_len	Yes	R/W	Packet
0x11E	crc_poly_0	Yes	R/W	Packet
0x11F	crc_poly_1	Yes	R/W	Packet
0x120	sync_control	Yes	R/W	Packet
0x121	sync_byte_0	Yes	R/W	Packet
0x122	sync_byte_1	Yes	R/W	Packet
0x123	sync_byte_2	Yes	R/W	Packet
0x124	tx_base_adr	Yes	R/W	Packet
0x125	rx_base_adr	Yes	R/W	Packet
0x126	packet_length_control	Yes	R/W	Packet
0x127	packet_length_max	Yes	R/W	Packet
0x128	static_reg_fix	Yes	R/W	reserved
0x129	address_match_offset	Yes	R/W	Packet
0x12A	address_length	Yes	R/W	Packet
0x12B to 0x13D	address filtering	Yes	R/W	Packet
0x13E	rx_synth_lock_time	Yes	R/W	PHY
0x13F	tx_synth_lock_time	Yes	R/W	PHY

Table 39. Modem Configuration Memory

Address (Hex)	Register	Retained in PHY_SLEEP	R/W
0x307	pa_level_mcr	No	R/W
0x30C	wuc_config_high	No	R/W
0x30D	wuc_config_low	No	R/W
0x30E	wuc_value_high	No	R/W
0x30F	wuc_value_low	No	R/W
0x310	wuc_flag_reset	No	R/W
0x311	wuc_status	No	R
0x312	rssi_readback	No	R
0x315	max_afc_range	No	R/W
0x319	image_reject_cal_config	No	R/W
0x322	chip_shutdown	No	R/W
0x325	powerdown_aux	No	R/W
0x327	adc_readback_high	No	R
0x328	adc_readback_low	No	R
0x329	silicon_rev0	No	R
0x32A	silicon_rev1	No	R
0x32B	silicon_rev2	No	R
0x32C	silicon_rev3	No	R
0x32D	battery_monitor_threshold_voltage	No	R/W
0x32E	ext_uc_clk_divide	No	R/W
0x32F	agc_clk_divide	No	R/W
0x336	interrupt_source_0	No	R
0x337	interrupt_source_1	No	R
0x338	calibration_control	No	R/W
0x339	calibration_status	No	R
0x33A	image_reject_calibration_status	No	R/W
0x345	rxbb_cal_calwrd_readback	No	R
0x346	rxbb_cal_calwrd_overwrite	No	RW
0x359	adc_config_low	No	R/W
0x35A	adc_config_high	No	R/W
0x35B	agc_ook_control	No	R/W
0x35C	agc_config	No	R/W
0x35D	agc_mode	No	R/W
0x35E	agc_low_threshold	No	R/W
0x35F	agc_high_threshold	No	R/W
0x360	agc_gain_status	No	R
0x372	frequency_error_readback	No	R
0x3CB	vco_band_ovrw_val	No	R/W
0x3CC	vco_ampl_ovrw_val	No	R/W
0x3D0	vco_cal_cfg	No	R/W
0x3D2	osc_and_doubler_config	No	R/W
0x3DA	vco_band_readback	No	R
0x3DB	vco_ampl_readback	No	R
0x3F8	analog_test_bus_six	No	R/W
0x3F9	rssi_tstmux_sel	No	R/W
0x3FA	gpio_configure	No	R/W
0x3FD	test_dac_gain	No	R/W

Table 40. Packet RAM Memory

Address	Register	R/W
0x000	var_command	R/W
0x001to 0x004	Silicon Revision code. 0x001= 0x70 0x002= 0x23 0x003=revision code MSByte 0x004= revision code LSByte Only valid on power up or wake up from PHY_SLEEP as communications processor will overwrite these values on exiting PHY_ON.	R
0x005 to 0x00B	reserved	R
0x00C	var_state	R
0x00D	var_tx_mode	R/W
0x00E to 0x00F	reserved	R

BBRAM REGISTER DESCRIPTION

Table 41. 0x100: interrupt_mask_0

Bit	Name	R/W	Description
[7]	interrupt_num_wakeups	R/W	Interrupt when the number_of_wakeups exceeds the number_of_wakeups_irq_threshold of the firmware timer 1: enabled; 0: disabled
[6]	interrupt_swm_rssi_det	R/W	Interrupt indicating that the RSSI threshold has been exceeded (Smart Wake Mode) 1: enabled; 0: disabled
[5]	interrupt_aes_done	R/W	Interrupt when an AES operation is complete 1: enabled; 0: disabled
[4]	interrupt_tx_eof	R/W	End of frame interrupt after packet transmission 1: enabled; 0: disabled
[3]	interrupt_address_match	R/W	Interrupt on receive address match 1: enabled; 0: disabled
[2]	interrupt_crc_correct	R/W	Interrupt on reception of valid CRC 1: enabled; 0: disabled
[1]	interrupt_sync_detect	R/W	Interrupt on reception of valid sync byte pattern 1: enabled; 0: disabledaddress_match
[0]	interrupt_premable_detect	R/W	Interrupt on receive preamble qualification 1: enabled; 0: disabled

Table 42. 0x101: interrupt_mask_1

Bit	Name	R/W	Description
[7]	battery_alarm	R/W	Interrupt on Battery voltage < user defined threshold 1: Enabled; 0: Disabled
[6]	cmd_ready	R/W	Interrupt on communications processor ready to accept a new command 1: Enabled; 0: Disabled
[5]	reserved	R/W	unused
[4]	wuc_timeout	R/W	Interrupt when the wuc timer reaches 0x0000 1: Enabled; 0: Disabled
[3]	reserved	R/W	unused
[2]	reserved	R/W	unused
[1]	spi_ready	R/W	Interrupt on SPI ready for access 1: Enabled; 0: Disabled
[0]	cmd_finished	R/W	Interrupt on command finished. 1: Enabled; 0: Disabled

Table 43. 0x102: number_of_wakeups_0

Bit	Name	R/W	Description
[7:0]	number_of_wakeups[7:0]	R/W	Bits [7:0] of [15:0] of an internal 16-bit count of the number of wake ups (wuc timeouts) the device has gone through. It can be initialized to 0x0000.

Table 44. 0x103: number_of_wakeups_1

Bit	Name	R/W	Description
[7:0]	number_of_wakeups[15:8]	R/W	Bits [15:8] of [15:0] of an internal 16-bit count of the number of WUC wake ups the device has gone through. It can be initialized to 0x0000.

Table 45. 0x104: number_of_wakeups_irq_threshold_0

Bit	Name	R/W	Description
[7:0]	number_of_wakeups_irq_threshold[7:0]	R/W	Bits [7:0] of [15:0]. This is the threshold for the number of wakeups (wuc timeouts). It is a 16-bit count threshold that is compared against the number_of_wakeups. When this threshold is exceeded the device

			wakes up into the state PHY_OFF and optionally generates interrupt_num_wakeups.

Table 46. 0x105: number_of_wakeups_irq_threshold_1

Bit	Name	R/W	Description
[7:0]	number_of_wakeups_irq_threshold[15:8]	R/W	Bits [15:8] of [15:0].

Table 47. 0x106: rx_dwell_time

Bit	Name	R/W	Description
[7:0]	rx_dwell_time	R/W	When the WUC is used and SWM is enabled), then the radio powers up and enables the receiver on the channel defined in the BBRAM and listens for this period of time. If no preamble pattern is detected in this period, the device goes back to sleep. Receive dwell time (s) = rx_dwell_time $\times \frac{6.5MHz}{128\times \text{parmtime\_divider}}$

Table 48. 0x107: parmtime_divider

Bit	Name	R/W	Description
[7:0]	parmtime_divider	R/W	Units of time used to define the rx_dwell_time time period. Timer tick rate = $\frac{128\times \text{parmtime\_divider}}{6.5MHz}$ A value of 0x33h will give clock of 995.7Hz or a period of 1.004ms

Table 49. 0x108: swm_rssi_thresh

Bit	Name	R/W	Description
[7:0]	swm_rssi_thresh	R/W	This sets the RSSI threshold when in Smart Wake Mode with RSSI detection enabled. Threshold (dBm) = swm_rssi_thresh - 107

Table 50. 0x109: channel_freq_0

Bit	Name	R/W	Description
[7:0]	channel_freq[7:0]	R/W	The RF channel frequency in Hz is set according to: $\text{Frequency (Hz)} = F_{PFD} \times \frac{(\text{channel\_freq}[23:0])}{2^{16}}$ where F_{PFD} is the PFD frequency and is equal to 26MHz.

Table 51. 0x10A: channel_freq_1

Bit	Name	R/W	Description
[7:0]	channel_freq[15:8]	R/W	refer to channel_freq_0 description

Table 52. 0x10B: channel_freq_2

Bit	Name	R/W	Description

[7:0]	channel_freq[23:16]	R/W	refer to channel_freq_0 description

Table 53. 0x10C: radio_cfg_0

Bit	Name	R/W	Description
[7:0]	data_rate[7:0]	R/W	The data rate in bps is set according to: $\text{Data Rate(bps)} = \text{data\_rate}[11:0] \times 100$

Table 54. 0x10D: radio_cfg_1

Bit	Name	R/W	Description
[7:4]	freq_deviation[11:8]	R/W	refer to freq_deviation description in radio_cfg_2
[3:0]	data_rate[11:8]	R/W	refer to data_rate description in radio_cfg_0

Table 55. 0x10E: radio_cfg_2

Bit	Name	R/W	Description
[7:0]	freq_deviation[7:0]	R/W	The binary level FSK frequency deviation in Hz (defined as frequency difference between carrier frequency and 1/0 tones) is set according to: $Frequency\ Deviation\ (Hz) = freq\_deviation[11:0] \times 100$

Table 56. 0x10F: radio_cfg_3

Bit	Name	R/W	Description
[7:0]	discrim_bw[7:0]	R/W	***Step 1: Calculate the discriminator bandwidth coefficient K*** The discriminator bandwidth coefficient K depends on the modulation index (MI) which is determined by: $MI = \frac{2 \times FSK\_dev}{datarate}$ Where FSK_dev is the FSK/GFSK frequency deviation in Hz, measured from the carrier to the one (+ deviation) or zero (- deviation frequency, and datarate is the data rate in bps. The value of K is then determined by: $MI \geq 1, \quad K = Floor\left[\frac{IF\_freq}{FSK\_dev + Freq\_error\_max}\right]$ $MI < 1, \quad K = Floor\left[\frac{IF\_freq}{\frac{datarate}{2} + Freq\_error\_max}\right]$ Where MI is the modulation index, K is the discriminator coefficient, Floor[] is a function to round down to the nearest integer, IF_freq is the IF frequency in Hz (200kHz or 300kHz), FSK_dev is the FSK/GFSK frequency deviation in Hz and Freq_error_max is the maximum expected frequency error, in Hz, between Tx and Rx. ***Step 2: Calculate the discrim_bw setting***

			The bandwidth setting of the discriminator is calculated based on the discriminator coefficient K and the IF frequency. The bandwidth is set using discrim_bw setting (location 0x10F) which is calculated according to: $discrim\_bw[7:0] = Round\left[\frac{K \times 3.25MHz}{IF\_freq}\right]$

Table 57. 0x110: radio_cfg_4

Bit	Name	R/W	Description
[7:0]	post_demod_bw[7:0]	R/W	The bandwidth of the post-demodulator bandwidth is given by: $post\_demod\_bw = Round[(7.5 \times 10^{-4} \times data\ rate(bps) \times 0.73) - 5]$

Table 58. 0x111: radio_cfg_5

Bit	Name	R/W	Description
[7:0]	reserved	R/W	Set to zero

Table 59. 0x112: radio_cfg_6

Bit	Name	R/W	Description
[7:2]	synth_lut_config_0	R/W	This holds the values for synth_int_cp_icode_nom and synth_lpf_cp_icode_nom which set the charge pump current of the PLL. In conjunction with setting synth_lut_control =1 or =3 this setting allows the receiver PLL loop bandwidth to be changed to optimize the receiver local oscillator phase noise.
[1:0]	discrim_phase[1:0]	R/W	The phase setting of the discriminator is calculated based on the discriminator coefficient K as described below. Refer to the discrim_bw for information on how to calculate K. **Table 60. Setting the discrim_phase[1:0] value based on K** K / K/2 / (K+1)/2 / discrim_phase[1:0] even / odd / - / 0 even / even / - / 1 odd / - / even / 2 odd / - / odd / 3

Table 61. 0x113: radio_cfg_7

Bit	Name	R/W	Description
[7:6]	agc_lock_mode	R/W	This set 0 : free running 1 : manual 2 : hold 3 : lock after preamble/sync word (only locks on sync word if preamble_match =0)
[5:4]	synth_lut_control	R/W	By default the synthesizer loop bandwidth is automatically selected from look up tables (LUT) in ROM memory. A narrow bandwidth is selected in receive to ensure optimum interference rejection, while in transmit the bandwidth is selected based on the data rate and modulation settings. For the majority of applications these

			automatically selected PLL loop bandwidths will be optimum. However, in some applications it may be necessary to use custom transmit or receive bandwidths in which case various options exist, as explained in Table 62. **Table 62. synth_lut_control options** **synth_lut_control** — **Description** 0 — Use pre-defined transmit and receive LUTs. The LUTs are automatically selected from ROM memory on transitioning into PHY_TX or PHY_RX. 1 — Use custom receive LUT based on synth_lut_config_0 and synth_lut_config_1. In transmit the pre-defined LUT in ROM is used. 2 — Use a custom transmit LUT. The custom transmit LUT needs to be written to packet RAM locations 0x10 to 0x18. In receive the pre-defined LUT in ROM is used. 3 — Use a custom receive LUT based on synth_lut_config_0 and synth_lut_config_1 and use a custom transmit LUT. The custom transmit LUT needs to be written to packet RAM locations 0x10 to 0x18. As packet RAM memory is lost in the PHY_SLEEP state the custom LUT for transmit needs to be re-loaded to packet RAM after waking from PHY_SLEEP.
[3:0]	synth_lut_config_1	R/W	This holds the values for lf_r2pi_res_code and lf_r2pl_res_code which control the value of the second pole resistor of the PLL loop filter. In conjunction with setting synth_lut_control =1 or =3 this setting allows the receiver PLL loop bandwidth to be changed to optimize the receiver local oscillator phase noise.

Table 63. 0x114: radio_cfg_8

Bit	Name	R/W	Description
[7]	pa_single_diff_sel	R/W	**pa_single_diff_sel** — **PA** 0 — Single-ended PA enabled 1 — Differential PA enabled
[6:3]	pa_power	R/W	Sets the PA power. Note pa_level_mcr = 4xpa_level + 3. **pa_power** — **PA level** 0000b — setting 3 0001b — setting 7 0010b — setting 11 : — : 1111b — setting 63

[2:0]	pa_ramp	R/W	Sets the PA ramp rate. The PA will ramp at the programmed rate until it reaches the level indicated by the pa_power setting. The ramp rate is dependent on the programmed data rate. **pa_ramp** / **Ramp rate** 000b: reserved 001b: 256 codes per bit 010b: 128 codes per bit 011b: 64 codes per bit 100b: 32 codes per bit 101b: 16 codes per bit 110b: 8 codes per bit 111b: 4 codes per bit To ensure optimum performance the PA ramp rate has a minimum value based on the data rate and the pa_level or pa_level_mcr settings. This minimum value is described by: $pa\_ramp[2:0] > 11 - \log_2\left[\frac{10000 \times pa\_mcr\_level[7:0]}{data\_rate[11:0]}\right]$ Where pa_mcr_level is related to the pa_level setting by pa_level_mcr = 4×pa_level + 3.

Table 64. 0x115: radio_cfg_9

Bit	Name	R/W	Description
[7:6]	ifbw	R/W	Sets the receiver IF filter bandwidth. Note that setting an IF filter bandwidth of 200kHz automatically changes the receiver IF frequency from 200kHz to 300kHz. **ifbw** / **IF bandwidth** 00: 100kHz 01: 150kHz 10: 200kHz 11: 300kHz
[5:3]	mod_scheme	R/W	Sets the transmitter modulation. **demod_scheme** / **Modulation Scheme** 000: 2-level FSK 001: 2-level GFSK 010: OOK 011: carrier only 100 to 111: reserved
[2:0]	demod_scheme	R/W	Sets the receiver demodulation scheme. **demod_scheme** / **Demodulation Scheme** 000: FSK 001: GFSK 010: OOK 011 to 111: reserved

Table 65. 0x116: radio_cfg_10

Bit	Name	R/W	Description
[7:5]	reserved	R/W	

[4]	afc_polarity	R/W	Set this to 1.
[3:2]	afc_scheme	R/W	Set this to 2.
[1:0]	afc_lock_mode	R/W	Sets the AFC mode. **afc_lock_mode** / **Mode** 00 – Free Running: AFC is free running 01 – Disabled: AFC is disabled 10 – Hold AFC: AFC is paused 11 – Lock: AFC locks after preamble or sync word (only locks on sync word if preamble_match =0)

Table 66. 0x117: radio_cfg_11

Bit	Name	R/W	Description
[7:4]	afc_kp	R/W	Sets the AFC PI controller proportional gain in FSK/GFSK and the recommended value is 0x3. In OOK modulation this setting is used to control the OOK threshold loop and the recommended value is 0x3. **afc_kp** / **proportional gain** 0000 – 2^0 0001 – 2^1 0010 – 2^2 : – : 1111 – 2^{15}
[3:0]	afc_ki	R/W	Sets the AFC PI controller integral gain in FSK/GFSK and the recommended value is 0x7. In OOK modulation this setting is used to control the OOK threshold loop and the recommended value is 0x6. **afc_ki** / **Intergral gain** 0000 – 2^0 0001 – 2^1 0010 – 2^2 : – : 1111 – 2^{15}

Table 67. 0x118: image_reject_cal_phase

Bit	Name	R/W	Description
[7]	reserved	R/W	
[6:0]	image_reject_cal_phase	R/W	**image_reject_cal_phase** / **I/Q Phase adjustment** 0000000 – 0 0000001 – 1 : – : 1111111 – 63

Table 68. 0x119: image_reject_cal_amplitude

Bit	Name	R/W	Description
[7]	reserved	R/W	
[6:0]	image_reject_cal_amplitude	R/W	**image_reject_cal_amplitude** / **I/Q Gain adjustment** 0000000 – 0 0000001 – 1

			:	:
			1111111	63

Table 69. 0x11A: mode_control

Bit	Name	R/W	Description
[7]	swm_en	R/W	1: Smart wake mode enabled 0: Smart wake mode disabled
[6]	bb_cal	R/W	1: IF Filter calibration enabled 0: IF Filter calibration disabled The IF filter calibrations is automatically performed on the transition form PHY_OFF to PHY_ON if this bit is set.
[5]	swm_rssi_qual	R/W	1: RSSI qualify in low power mode enabled 0: RSSI qualify in low power mode disabled
[4]	tx_auto_turnaround	R/W	1: Fast PHY_TX to PHY_RX switching enabled 0: Fast PHY_TX to PHY_RX switching disabled
[3]	rx_auto_turnaround	R/W	1: Fast PHY_RX to PHY_TX switching enabled 0: Fast PHY_RX to PHY_TX switching disabled
[2]	custom_trx_synth_lock_time_en	R/W	1: Use the custom synthesizer lock time defined in register 0x3E and 0x3F 0: default synthesizer lock time
[1]	ext_lna_en	R/W	1: External LNA enable signal on ATB4 is enabled. The signal is logic high while the ADF7023 is in the PHY_RX state and logic low while in any other non-sleep state. 0: External LNA enable signal on ATB4 is disabled.
[0]	ext_pa_en	R/W	1: External PA enable signal on ATB3 is enabled. The signal is logic high while the ADF7023 is in the PHY_TX state and logic low while in any other non-sleep state. 0: External PA enable signal on ATB3 is disabled.

Table 70. 0x11B: preamble_match

Bit	Name	R/W	Description	
[7:4]	reserved	R/W		
[3:0]	preamble_match	R/W	**preamble_match**	**Description**
			0x0C	0 errors allowed
			0x0B	1 erroneous bit-pair allowed in 12 bit-pairs
			0x0A	2 erroneous bit-pairs allowed in 12 bit-pairs
			0x09	3 erroneous bit-pairs allowed in 12 bit-pairs
			0x08	4 erroneous bit-pairs allowed in 12 bit-pairs
			0x00	Preamble detection disabled

Table 71. 0x11C: symbol_mode

Bit	Name	R/W	Description
[7]	reserved	R/W	

[6]	manchester_enc	R/W	1: Manchester encoding and decoding enabled 0: Manchester encoding and decoding disabled
[5]	prog_crc_en	R/W	1: Programmable CRC enabled 0: Programmable CRC disabled
[4]	eight_ten_enc	R/W	1: 8b/10b encoding and decoding enabled 0: 8b/10b encoding and decoding disabled
[3]	data_whitening	R/W	1: Data whitening and de-whitening enabled 0: Data whitening and de-whitening disabled
[2:0]	symbol_length	R/W	**symbol_length** | 000 | 8 bit (recommended except when 8b/10b is being used) 001 | 10 bit (for 8b/10b encoding) 010 | reserved : | : 111 | reserved

Table 72. 0x11D: preamble_len

Bit	Name	R/W	Description
[7:0]	preamble_len	R/W	Length of preamble in bytes. Example a value of decimal 3 results in a preamble of 24 bits.

Table 73. 0x11E: crc_poly_0

Bit	Name	R/W	Description
[7:0]	crc_poly[7:0]	R/W	Lower byte of crc_poly[15:0], which sets the CRC polynomial.

Table 74. 0x11F: crc_poly_1

Bit	Name	R/W	Description
[7:0]	crc_poly[15:8]	R/W	Upper byte of crc_poly[15:0] which sets the CRC polynomial. Refer to the Packet Mode section for further details on how to configure a CRC polynomial

Table 75. 0x120: sync_control

Bit	Name	R/W	Description
[7:6]	sync_error_tol	R/W	Sets the sync word error tolerance in bits. **sync_error_tol** | **Bit error tolerance** 00 | 0 bit errors allowed 01 | 1 bit error allowed 10 | 2 bit error allowed 11 | 3 bit error allowed
[5]	reserved	R/W	

[4:0]	sync_word_length	R/W	Sets the sync word length in bits. 24 bits is the maximum. Note that the sync word matching length can be any value up to 24 bits, but the transmitted sync word pattern is a multiple of 8 bits. Hence, for non-byte-length sync words, the transmitted sync pattern should be filled out with the preamble pattern. **sync_word_length** / **Length in bits** 0 / 0 1 / 1 : / : 24 / 24

Table 76. 0x121: sync_byte_0

Bit	Name	R/W	Description
[7:0]	sync_byte[7:0]	R/W	Lower byte of sync word pattern. The sync word pattern is transmitted most significant bit first starting with sync_byte[7:0]. For non-byte length sync words the reminder of the least significant byte should be stuffed with preamble. If sync_word_length length is >16 bits then sync_byte_0, sync_byte_1 and sync_byte_2 are all transmitted for a total of 24 bits. If sync_word_length is between 8 and 15 then sync_byte_1 and sync_byte_2 are transmitted. If sync_word_length is between 1 and 7 then sync_byte_2 is transmitted for a total of 8 bits. If the sync word length is 0 then no sync bytes are transmitted.

Table 77. 0x122: sync_byte_1

Bit	Name	R/W	Description
[7:0]	sync_byte[15:8]	R/W	Mid byte of sync word pattern.

Table 78. 0x123: sync_byte_2

Bit	Name	R/W	Description
[7:0]	sync_byte[23:16]	R/W	Upper byte of sync word pattern.

Table 79. 0x124: tx_base_adr

Bit	Name	R/W	Description
[7:0]	tx_base_adr	R/W	Address in Packet RAM of transmit packet. This address indicates to the comms processor the location of the first byte of the transmit packet

Table 80. 0x125: rx_base_adr

Bit	Name	R/W	Description
[7:0]	rx_base_adr	R/W	Address in Packet RAM of receive packet. The communications processor will write any qualified received packet to Packet RAM, starting at this memory location.

Table 81. 0x126: packet_length_control

Bit	Name	R/W	Description
[7]	data_byte	R/W	Over the air arrangement of each transmitted Packet RAM byte. Byte transmitted either MSB or LSB first. The same setting should be used on the Tx and Rx side of the link. 1: Data byte MSB first 0: Data byte LSB first
[6]	packet_len	R/W	1: Fixed packet length mode. Fixed packet length in tx and rx, given by packet_lenght_max. 0: Variable packet length mode. In rx mode packet length is given by first byte in Packet RAM. In tx mode the packet length is given by packet_lenght_max.
[5]	crc_en	R/W	1: Append CRC in transmit mode. Check CRC in receive mode. 0: No CRC addition in transmit mode. No CRC check in receive mode.
[4:3]	data_mode	R/W	Sets the ADF7023 to packet mode or SPORT mode for transmit and receive data. **data_mode** / **Description** 0 / Packet Mode enabled 1 / SPORT mode enabled. GP4 interrupt enabled on preamble detection. Rx Data enabled on preamble detection. 2 / SPORT mode enabled. GP4 interrupt enabled on sync word detection. Rx Data enabled on preamble detection. 3 / unused
[2:0]	length_offset	R/W	Offset value in bytes that is added to the received packet length field value (in variable length packet mode) so the communications processor knows the correct number of bytes to read. Useful in legacy systems where the definition of the packet length may or may not include CRC. **length_offset** / **bytes** 0 / -4 1 / -3 2 / -2 3 / -1 4 / 0 5 / +1 6 / +2 7 / +3

Table 82. 0x127: packet_length_max

Bit	Name	R/W	Description
[7:0]	packet_length_max	R/W	If variable packet length mode is used (packet_len_control = 0), then packet_length_max sets the maximum packet length in bytes. If fixed packet length mode is used (packet_len_control = 1), then packet_length_max sets the length of the fixed packet in bytes. Note that the packet length is defined as the number of bytes from the end of the sync word to the start of the CRC. It also does not include the length_offset value

Table 83. 0x128: static_reg_fix

Bit	Name	R/W	Description
[7:0]	reserved	R/W	Set to 0x00

Table 84. 0x129: address_match_offset

Bit	Name	R/W	Description
[7:0]	address_match_offset	R/W	Location of first byte of address information in packet RAM

Table 85. 0x12A: address_length

Bit	Name	R/W	Description
[7:0]	address_length	R/W	Number of bytes in each address field (N_{ADR})

Table 86. 0x12B to 0x13D: address filtering

Address	Bit	R/W	Description
0x12B	[7:0]	R/W	Address match byte 0
0x12C	[7:0]	R/W	Address mask byte 0
0x12D	[7:0]	R/W	Address match byte 1
0x12E	[7:0]	R/W	Address mask byte 1
:			:
	[7:0]	R/W	Address Match byte N_{ADR}-1
	[7:0]	R/W	Address Mask byte N_{ADR}-1
	[7:0]	R/W	0x00 to end or N_{ADR} for another address check sequence.

Table 87. 0x13E: rx_synth_lock_time

Bit	Name	R/W	Description
[7:0]	rx_synth_lock_time	R/W	Allows the use of a custom synthesizer lock time counter in receive mode in conjunction with the custom_trx_synth_lock_time_en setting in the mode_control register. Applies after VCO calibration is complete. 2us step.

Table 88. 0x13F: tx_synth_lock_time

Bit	Name	R/W	Description
[7:0]	tx_synth_lock_time	R/W	Allows the use of a custom synthesizer lock time counter in transmit mode in conjunction with the custom_trx_synth_lock_time_en setting in the mode_control register. Applies after VCO calibration is complete. 2us step.

MCR REGISTER DESCRIPTION

Note that the MCR register settings are not retained when the device enters PHY_SLEEP.

Table 89. 0x307 pa_level_mcr

Bit	Name	R/W	Reset	Description
[5:0]	pa_level_mcr	R/W	0x0	Power amplifier Level. If PA Ramp is enabled the PA will ramp to this target level. The PA level can be set in the range 0 to 63. The PA level (with less resolution) can also be set via the BBRAM so the MCR setting should only be used if more resolution is required.

Table 90. 0x30C: wuc_config_high

Bit	Name	R/W	Reset	Description
[7]	reserved	W	0x0	Set to 0
[6]	wuc _bgap	W	0x0	Set to 0
[5]	wuc _ldo_synth	W	0x0	Set to 0
[4]	wuc _ldo_dig	W	0x0	Set to 0
[3]	wuc_xto26m_en	W	0x0	Set to 0
[2:0]	wuc _prescaler	W	0x0	

wuc_prescaler	32.768kHz Divider	Tick Period
000	1	30.52us
001	4	122.1us
010	8	244.1us
011	16	488.3us
100	128	3.91ms
101	1034	31.25ms
110	8192	250ms
111	65536	2000ms

Note that Register wuc_config_low should never be written to without updating Register wuc_config_high first.

Table 91. 0x30D: wuc_config_low

Bit	Name	R/W	Reset	Description
[7]	reserved	W	0x0	Set to 0
[6]	wuc _rcosc_en	W	0x0	1: enable; 0: disable RCOSC32K
[5]	wuc _xosc32k_en	W	0x0	1: enable; 0: disable XOSC32K
[4]	wuc _clksel	W	0x0	Select WUC timer clock source: 1: RC 32.768 kHz oscillator; 0: external crystal oscillator
[3]	wuc _bbram_en	W	0x0	1: enable; 0: disable power to BBRAM during PHY_SLEEP
[2:1]	reserved	W	0x0	Set to 0
[0]	wuc_arm	W	0x0	1: enable; 0: disable wake-up on WUC timeout event

Note that updates to Register wuc_value_high become effective only after Register wuc_value_low has been written to.

Table 92. 0x30E: wuc_value_high

Bit	Name	R/W	Reset	Description
[7:0]	wuc_timer_value[15:8]	W	0x0	WUC timer reload value, Bits[15:8] of [15:0]. A wake-up event is triggered when the WUC unit has been enabled and the timer has counted down to 0. The timer is clocked with the prescaler output rate. An update to this register becomes effective only after wuc_value_low is written.

Note that Register wuc_value_low should never be written to without updating register wuc_value_high first.

Table 93. 0x30F: wuc_value_low

Bit	Name	R/W	Reset	Description
[7:0]	wuc_timer_value[7:0]	W	0x0	WUC timer reload value, Bits[7:0] of [15:0]. A wake-up event is triggered when the WUC unit has been enabled and the timer has counted down to 0. The timer is clocked with the prescaler output rate.

Table 94. 0x310: wuc_flag_reset

Bit	Name	R/W	Reset	Description
[1]	wuc_rcosc_cal_en	R/W	0x0	1: enable; 0: disable rcosc32k calibration
[0]	wuc_flag_reset	R/W		1: reset the wuc_tmr_prim_toflag and wuc_porflag bits 0: normal operation

Table 95. 0x311: wuc_status

Bit	Name	R/W	Reset	Description
[7]	reserved	R	0x0	Reserved
[6]	wuc_rcosc_cal_error	R	0x0	1: RCOSC32K calibration exited with error 0: without error (only valid if wuc_rcosc_cal_en = 1)
[5]	wuc_rcosc_cal_ready	R	0x0	1: RCOSC32K calibration finished 0: in progress (only valid if wuc_rcosc_cal_en = 1)
[4]	xosc32k_rdy	R	0x0	1: XOSC32K oscillator has settled 0: not settled (only valid if wuc_config_low_xosc32k_en = 1)
[3]	xosc32k_out	R	0x0	Output signal of XOSC32K oscillator (instantaneous)
[2]	wuc_porflag	R	0x0	1: chip cold start event has been registered 0: not registered
[1]	wuc_tmr_prim_toflag	R	0x0	1: WUC timeout event has been registered 0: not registered (the output of a latch triggered by a timeout event)
[0]	wuc_tmr_prim_toevent	R	0x0	1: WUC timeout event is present 0: not present (this bit is set when the counter has reached 0; it is not latched)

Table 96. 0x312: rssi_readback

Bit	Name	R/W	Reset	Description
[7:0]	rssi_readback	R	0x0h	Receive input power. After reception of a packet the rssi_readback value is valid. RSSI (dBm) = rssi_readback -107

Table 97. 0x315: max_afc_range

Bit	Name	R/W	Reset	Description
[7:0]	max_afc_range	R/W	0x32	Limits the AFC pull-in range. Automatically set by the communications processor on transitioning into PHY_RX to be equal to half the IF bandwidth. Example, IF bandwidth = 200kHz, AFC pull in range = ±100 kHz.

Table 98. 0x319: image_reject_cal_config

Bit	Name	R/W	Reset	Description
[7:6]	reserved	R/W	0x0	
[5]	image_reject_cal_ovwrt_en	R/W	0x0	Overwrite control for image reject calibration results
[4:3]	image_reject_frequency	R/W	0x0	Set the fundamental frequency of the IR calibration source 00: IR calibration source disabled in XTAL divider 01: RF calibration frequency = XTAL/4 10: RF calibration frequency = XTAL/8 11: RF calibration frequency = XTAL/16
[2:0]	image_reject_power	R/W	0x0	Set power level of IR Cal source 000: IR calibration source disabled at mixer input

				001: power level = min 010: power level = min 011: power level = min × 2 100: power level = min × 2 101: power level = min × 3 110: power level = min × 3 111: power level = min × 4

Table 99. 0x322: chip_shutdown

Bit	Name	R/W	Reset	Description
[7:6]	reserved	R/W	0x0	
[0]	chip_shtdn_req	R/W	0x0	WUC chip state control flag. 0: remain in active state. 1: invoke chip shutdown. Note that CSN must also be high to initiate a shutdown.

Table 100. 0x325: powerdown_aux

Bit	Name	R/W	Reset	Description
[7:2]	reserved	R/W	0x0	
[1]	tempmon_pd_en	R/W	0x0	1: enable; 0: disable temperature monitor
[0]	battmon_pd_en	R/W	0x0	1: enable; 0: disable battery monitor

Table 101. 0x327: adc_readback_high

Bit	Name	R/W	Reset	Description
[7:5]	reserved	R	0x0	Ignore
[4:0]	adc_readback[7:3]	R	0x0	ADC readback MSBs

Table 102. 0x328: adc_readback_low

Bit	Name	R/W	Reset	Description
[7:5]	adc_readback[2:0]	R	0x0	ADC readback LSBs
[4:0]	reserved	R	0x0	Ignore

Table 103. 0x329: silicon_rev0

Bit	Name	R/W	Reset	Description
[7:0]	silicon_revision_code[7:0]	R	0x0	Silicon revision bits[7:0]

Table 104. 0x32A: silicon_rev1

Bit	name	R/W	Reset	Description
[7:0]	silicon_revision_code[15:8]	R	0x0	Silicon revision bits[15:8]

Table 105. 0x32B: silicon_rev2

Bit	Name	R/W	Reset	Description
[7:0]	silicon_revision_code[23:16]	R	0x0	Silicon revision bits[23:16]

Table 106. 0x32C: silicon_rev3

Bit	Name	R/W	Reset	Description
[7:0]	silicon_revision_code[31:24]	R	0x0	Silicon revision bits[31:24]

Table 107. 0x32D: battery_monitor_threshold_voltage

Bit	Name	R/W	Reset	Description
[7:5]	reserved	R/W	0x0	
[4:0]	battmon_voltage	R/W	0x0	Battery monitor threshold voltage sets the alarm level for the battery monitor. The alarm is raised by the interrupt. Battery monitor trip voltage, V_{TRIP} = 1.7 V + 62 mV × *battmon_voltage*

Table 108. 0x32E: ext_uc_clk_divide

Bit	Name	R/W	Reset	Description
[7:4]	reserved	R/W	0x0	
[3:0]	ext_uc_clk_divide	R/W	0x4	Optional output clock frequency on GP5 Output Frequency = XTAL/ext_uc_clk_divide To disable, set ext_uc_clk_divide = 0.

Table 109. 0x32F: agc_clk_divide

Bit	Name	R/W	Reset	Description
[7:0]	agc_clock_divide	R/W	0x28	AGC Clk Divider for G/FSK mode. The AGC rate is (26MHz/(16*agc_clk_divide))

Table 110. 0x336: interrupt_source_0

Bit	Name	R/W	Reset	Description
[7]	interrupt_num_wakeups	R	0x0h	The number of WUC wakeups (number_of_wakeups[15:0]) has reached the threshold (number_of_wakeups_irq_threshold[15:0])
[6]	interrupt_swm_rssi_det	R	0x0h	RSSI above threshold interrupt (Smart Wake Mode)
[5]	interrupt_aes_done	R	0x0h	AES encryption/decryption complete interrupt
[4]	interrupt_tx_eof	R	0x0h	Packet transmission finished interrupt
[3]	interrupt_address_match	R	0x0h	Packet with address match interrupt
[2]	interrupt_crc_correct	R	0x0h	Packet with correct CRC interrupt
[1]	interrupt_sync_detect	R	0x0h	Sync word detection interrupt
[0]	interrupt_preamble_detect	R	0x0h	Preamble detection interrupt

Table 111. 0x337: interrupt_source_1

Bit	Name	R/W	Reset	Description
[7]	battery_alarm	R/W	0x0	Battery voltage dropped below user set threshold value.
[6]	cmd_ready	R/W	0x0	Communications processor ready to accept a new command
[5]	unused	R/W	0x0	
[4]	wuc_timeout	R/W	0x0	Wake-up timer has timed out.
[3]	interrupt_rtc_clock	R/W	0x0	RTC interrupt.
[2]	unused	R/W	0x0	
[1]	spi_ready	R/W	0x0	SPI ready for access.
[0]	cmd_finished	R/W	0x0	command has finished.

Table 112. 0x338: calibration_control

Bit	Name	R/W	Reset	Description
[7:2]	reserved	R/W	0x0	
[1]	synth_cal_en	R/W	0x0	1: enable; 0: disables the synthesizer calibration state machine
[0]	rxbb_cal_en	R/W	0x0	1: enable; 0: disable receiver baseband filter (RXBB) calibration

Table 113. 0x339: calibration_status

Bit	Name	R/W	Reset	Description
[7:3]	reserved	R	0x0	
[2]	pa_ramp_finished	R	0x0	
[1]	synth_cal_ready	R	0x0	1: synthesizer calibration finished successfully 0: synthesizer calibration in progress
[0]	rxbb_cal_ready	R	0x0	Receive IF filter calibration 1: complete 0: in progress (valid while Rxbb_Cal_En = 1)

Table 114. 0x33A: image_rejection_cal_status

Bit	Name	R/W	Reset	Description
[0]	ir_cal_ready	R/W	0x1	

Table 115. 0x345: rxbb_cal_calwrd_readback

Bit	Name	R/W	Reset	Description
[5:0]	rxbb_cal_calwrd	R	0x0	RXBB reference oscillator calibration word. Valid after RXBB calibration cycle has been completed. 6 LSBs

Table 116. 0x346: rxbb_cal_calwrd_overwrite

Bit	Name	R/W	Reset	Description
[6:1]	rxbb_cal_dcalwrd_ovwrt_in	RW	0	RXBB reference oscillator calibration overwrite word.
[0]	rxbb_cal_dcalwrd_ovwrt_en	RW	0	1=enable / 0=disable RXBB reference oscillator calibration word overwrite mode

Table 117. 0x359: adc_config_low

Bit	Name	R/W	Reset	Description
[7:6]	adc_acquisition	R/W	0x0	00: 4 clock cycles for acquisition (default) 01: 6 clock cycles for acquisition 10: 10 clock cycles for acquisition 11: 18 clock cycles for acquisition
[5:4]	adc_resolution	R/W	0x0	00: 12 bits (default) 01: 10 bits 10: 13 bits 11: 13 bits
[3:2]	adc_ref_chsel	R/W	0x0	00: RSSI (default) 01: external AIN 10: temperature sensor 11: unused
[1:0]	adc_reference_control	R/W	0x0	The following reference values are valid for a 3 V supply: 00: 1.85 V (default) 01: 1.95 V 10: 1.75 V 11: 1.65 V

Table 118. 0x35A: adc_config_high

Bit	Name	R/W	Reset	Description
[7]	reserved	R/W	0x0	
[6:5]	filtered_adc_mode	R/W	0x0	Filtering modes: 00: normal operation (no filter) 01: unfiltered AGC loop, filtered readback (updated upon MCR read, either by SPI or packet_handler) 10: unfiltered AGC loop, filtered readback (update at AGC clock rate) 11: filtered AGC loop, filtered readback
[4]	adc_ext_ref_enb	R/W	0x1	Bring low to power down ADC reference
[3:0]	adc_analog_clk_divide	R/W	0x1	ADC clock frequency divider

Table 119. 0x35B: agc_ook_control

Bit	Name	R/W	Reset	Description
[5:3]	ook_agc_clk_trk	R/W	0x2	AGC update rate during tracking phase: $AGC\ update\ rate = \frac{Fman}{2^{(ook\_agc\_clk\_trk\ +1)}}$ where Fman = the manchester symbol rate. Manchester encoding is recommended for OOK Note: ook_agc_clk_trk must be > = ook_agc_clk_acq
[2:0]	ook_agc_clk_acq	R/W	0x1	AGC update rate during acquisition phase:

				$AGC\ update\ rate = \frac{Fman}{2^{(ook\_agc\_clk\_acq\ +1)}}$ where Fman = the manchester symbol rate. Manchester encoding is recommended for OOK. Note: ook_agc_clk_trk must be > = ook_agc_clk_acq

Table 120. 0x35C: agc_config

Bit	Name	R/W	Reset	Description
[7:6]	lna_gain_change_order	R/W	0x2	LNA gain change order
[5:4]	mixer_gain_change_order	R/W	0x1	Mixer gain change order
[3:2]	filter_gain_change_order	R/W	0x3	Filter gain change order
[1]	allow_extra_lo_lna_gain	R/W	0x0	Allow extra Low LNA gain setting
[0]	disallow_max_gain	R/W	0x0	Disallow max AGC gain setting

Table 121. 0x35D: agc_mode

Bit	Name	R/W	Reset	Description
[7]	reserved	R/W	0x0	
[6:5]	agc_operation_mcr	R/W	0x0	00: free running AGC 01: manual AGC 10: freeze AGC 11: lock AGC after preamble
[4:3]	lna_gain	R/W	0x0	00: low 01: medium 10: high 11: reserved
[2]	mixer_gain	R/W	0x0	0: low 1: high
[1:0]	filter_gain	R/W	0x0	00: low 01: medium 10: high 11: reserved

Table 122. 0x35E: agc_low_threshold

Bit	Name	R/W	Reset	Description
[7:0]	agc_low_threshold	R/W	0x37	AGC low threshold

Table 123. 0x35F: agc_high_threshold

Bit	Name	R/W	Reset	Description
[7:0]	agc_high_threshold	R/W	0x69	AGC high threshold

Table 124. 0x360: agc_gain_status

Bit	Name	R/W	Reset	Description
[7:5]	reserved	R	0x0	
[4:3]	lna_gain_readback	R	0x0	00: low 01: medium 10: high 11: reserved
[2]	mixer_gain_readback	R	0x0	0: low 1: high
[1:0]	filter_gain_readback	R	0x0	00: low 01: medium 10: high 11: reserved

Table 125. 0x372: frequency_error_readback

Bit	Name	R/W	Reset	Description
[7:0]	frequency_error_readback	R	0x0	Frequency error between received signal frequency and receive channel frequency = frequency_error_readback × 1kHz. The most significant bit of frequency_error_readback determines the sign of the offset.

Table 126. 0x3CB: vco_band_ovrw_val

Bit	Name	R/W	Reset	Description
[7:0]	vco_band_ovrw_val	R/W	0x0	Overwrite value for the VCO frequency band. Active when vco_band_ovrw_en = 1

Table 127. 0x3CC: vco_ampl_ovrw_val

Bit	Name	R/W	Reset	Description
[7:0]	vco_ampl_ovrw_val	R/W	0x0	Overwrite value for the VCO bias current DAC. Active when vco_ampl_ovrw_en= 1

Table 128. 0x3CD: vco_ovrw_en

Bit	Name	R/W	Reset	Description
[7:6]	reserved	R/W	0x0	reserved
[5:2]	vco_q_amp_ref	R/W	0x0	VCO amplitude level control reference DAC during Q phase.
[1]	vco_ampl_ovrw_en	R/W	0x0	1:Enable, 0:Disable VCO bias current DAC overwrite
[0]	vco_band_ovrw_en	R/W	0x0	1:Enable, 0:Disable VCO frequency band overwrite

Table 129. 0x3D0: vco_cal_cfg

Bit	Name	R/W	Reset	Description
[7:4]	reserved	R/W	0x0	reserved
[3:0]	vco_cal_cfg	R/W	0x1	VCO calibration state machine configuration. Set vco_cal_cfg = 0xF to bypass the VCO calibration on the PHY_TX and PHY_RX transitions. Set vco_cal_cfg = 0x1 to enable the VCO calibrations on these transitions.

Table 130. 0x3D2: osc_and_doubler_config

Bit	Name	R/W	Reset	Description
[7:6]	reserved	R/W	0x0	Write 0
[5:3]	xosc_cap_dac	R/W	0x0	26 MHz crystal oscillator (XOSC26N) tuning capacitor control word
[2:0]	reserved	R/W	0x0	Write 0

Table 131. 0x3DA: vco_band_readback

Bit	Name	R/W	Reset	Description
[7:0]	vco_band_readback	R	0x0	Read-back of the VCO bias current DAC after calibration

Table 132. 0x3DB: vco_ampl_readback

Bit	Name	R/W	Reset	Description
[7:0]	vco_ampl_readback	R	0x0	Read-back of the VCO bias current DAC after calibration

0x3F8: analog_test_bus_six

Bit	Name	R/W	Reset	Description
[7:0]	analog_test_bus_six	R/W	0x0	To enable analog RSSI on ATB3 set analog_test_bus_six =0x64 in conjunction with setting rssi_tstmux_sel = 0x3.

0x3F9: rssi_tstmux_sel

Bit	Name	R/W	Reset	Description
[7]	reserved	R/W	0x0	
[6:2]	reserved	R/W	0x0	
[1:0]	rssi_tstmux_sel	R/W	0x0	To enable analog RSSI on ATB3 set rssi_tstmux_sel = 0x3 in conjunction with setting analog_test_bus_six =0x64.

Table 133. 0x3FA: gpio_configure

Bit	Name	R/W	Reset	Description
[7:0]	gpio_configure	R/W	0x0	0x00: default 0x21: Slicer output on GP0 (i.e. bypass CDR) 0x40: Limiter outputs on GP0(Q) and GP1(I) 0x40: Filtered Limiter outputs on GP0(Q) and GP1(I) and un-filtered limiter outputs on GP2(Q) and GP3(I) 0x50: transmit data from packet handler on GP0 0x53: PA ramp finished on GP0 0xA0: SPORT mode 0 0xA1: SPORT mode 1 0xA2: SPORT mode 2 0xA3: SPORT mode 3 0xA4: SPORT mode 4 0xA5: SPORT mode 5 0xA6: SPORT mode 6 0xA6: SPORT mode 7 0xC9: Test DAC output on GP0

0x3FD: test_dac_gain

Bit	Name	R/W	Reset	Description
{7:4}	reserved	R/W	0x0	reserved
[3:0]	test_dac_gain	R/W	0x4	Set test_dac_gain = 0x0 when using the test DAC

OUTLINE DIMENSIONS

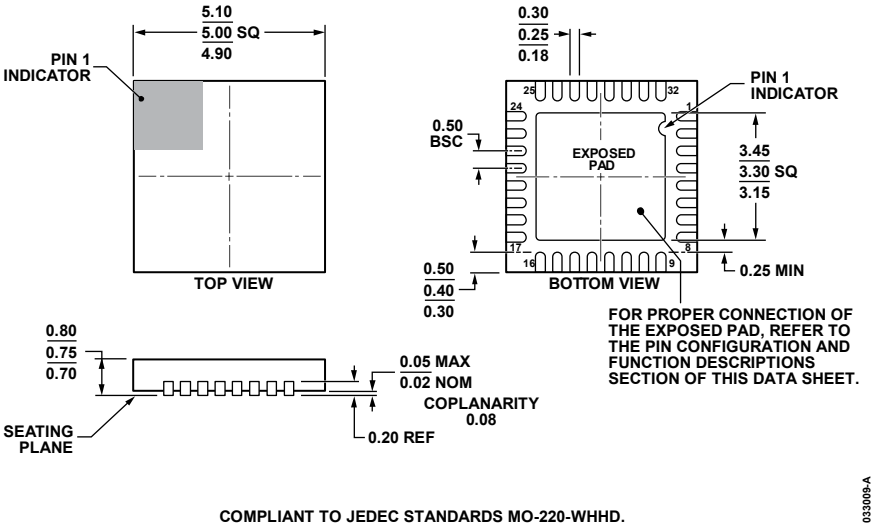


Figure 64. 32-Lead Lead Frame Chip Scale Package [LFCSP_WQ] , 5 mm × 5 mm Body, Very Very Thin Quad (CP-32-13)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADF7023BCPZ	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-13
ADF7023BCPZ-REEL	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-13
EVAL-ADF7XXXMB3Z		Evaluation Board (USB Mother Board)	
EVAL-ADF7023DBZ1		Evaluation Board (RF Daughter Board)	
EVAL-ADF7023DBZ2		Evaluation Board (RF Daughter Board)	

[1] Z = RoHS Compliant Part.

PR08291-0-4/10(PrF)

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